VLSI PHYSICAL DESIGN-I

Course Code	**: 20NHOP625A**	**Credits**	**: 3**
L:T:P:S	**: 3:0:0:0**	**CIE Marks**	**: 50**
Exam Hours	**: 03**	**SEE Marks**	**: 50**

Course Outcomes: At the end of the Course, the student will be able to:

CO1	Analyze the pre-requisites required for back-end VLSI design flow and its implementations
CO2	Gain sufficient practical knowledge on LINUX, GVIM editor usage and apply the scripting skills for the VLSI tools
CO3	Understand VLSI Synthesis and Evaluate the functionality of RTL and netlist
CO4	Understand timing analyses at various process and environment
CO5	Apply the learnt concepts of STA to evaluate the delay of the circuits.
CO6	Engage in independent learning and perform the timing and power report analysis

Mapping of Course Outcomes to Program Outcomes

	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PO12**
CO1	3	2	3	1	3	1	1	-	1	-	1	1
CO2	3	2	2	2	3	-	-	-	1	-	1	1
CO3	3	2	2	2	3	1	1	-	1	-	1	1
CO4	3	2	3	3	3	1	2	-	1	-	1	1
CO5	3	2	3	3	3	1	2	-	1	-	1	1
CO6	3	2	3	3	3	1	3	1	1	-	1	1

Module No	Module Contents	Hours	COs
1	**GVIM Editor**: GVIM Introduction, Features of GVIM, Create new file, Open file in Read-Only mode, Edit existing file, Basic modes, Insert, Append, Open new line, Substitute, Change, Replace, Join, VIM Navigating, Buffer, Swap files, Cut, copy, delete, paste actions, Undo and redo actions, Search settings , Search in current file ,Search in multiple files , Search in help files, Working with multiplefiles,buffers,Markers,Macros,Diff,Recording,Remote file editing Ref 2, Chapter 1,2,3,4,9,11,12,13,14,16	9	**CO1,CO2**
2	**Basics of Linux:** Linux commands, File management, Directories, File Permission, Basic utilities. Pipes and filters, Processes, Communication, shell scripting, Advanced Linux : Regular expressions, File system Basics **TCL :**Basic syntax, Commands, Operators, Loops, Arrays, Strings, Lists, Procedures, Packages, Files I/O, Regular expressions Text 1, Chapter 2,3,11 Reference 3, Chapter: 1,5,6,8,9	9	**CO1,CO2**
3	**Logic Synthesis:** Introduction to Logic Synthesis, Goals of Synthesis, Synthesis Flow, Input and Output of Synthesis Reference 4	9	**CO1,CO3**
4	**Introduction to STA:** Nanometer Designs, What is Static Timing Analysis? Why Static Timing Analysis?, Crosstalk and Noise, Design Flow, CMOS Digital Designs, FPGA Designs, Asynchronous Designs, STA at Different Design Phases, Limitations of Static Timing Analysis, Power Considerations, Reliability Considerations Text 3: Chapter 1	9	**CO4**
5	**STA Concepts:**Standard Cells, Propagation Delay, Slew of a Waveform, Skew between Signals, Timing Arcs and Unateness, Min and Max Timing Paths, Timing Modeling, Wireload Models,Crosstalk Glitch analysis, Configuring STA Environment, Setup and Hold Timing Check	9	**CO5 and CO6**

	Text 3:2.1.3,2.4,2.5,2.6,2.7,2.8,3.2,4.2,6.2,7.2,8.1 and 8.2		

TEXT BOOKS:

1. Beginning Linux Programming, 4th Edition, N.Matthew, R.Stones,Wrox, Wiley India Edition.
2. Richard Peterson, "Linux: The Complete Reference", sixth edition, Mc-Graw Hill, 2008
3. J. Bhasker, R Chadha, "Static Timing Analysis for Nanometer Designs: A Practical Approach", Springer, 2009

REFERENCE BOOKS:

1. Sridhar Gangadharan, Sanjay Churiwala, "Constraining Designs for Synthesis and Timing Analysis – A Practical Guide to Synopsis Design Constraints (SDC)", Springer, 2013.
2. https://www.iopb.res.in/vimbook-OPL.pdf
3. **https://www.ee.columbia.edu/~shane/projects/sensornet/part1.pdf**
4. **https://www.vlsi-backend-adventure.com/logic_synthesis.html**
5. **https://www.ee.columbia.edu/~shane/projects/sensornet/part1.pdf**

Mapping of CO v/s PSO:

Cos	PSO1	PSO2
	PHYSICAL DESIGN-I IN VLSI	
CO1	2	3
CO2	2	3
CO3	2	3
CO4	2	3
CO5	2	2
CO6	2	3

Assessment Pattern

CIE- Continuous Internal Evaluation

Theory (50 Marks)

Bloom's Taxonomy	Tests	Assignments	Quizzes	Co-curricular Activities
Marks	**25**	**10**	**5**	**10**
Remember	5	-	-	-
Understand	5	-	-	-
Apply	5	5	5	5
Analyze	10	-	-	-
Evaluate	-	-	-	5
Create	-	5	-	-

SEE- Semester End Examination

Theory (50 Marks)

Bloom's Taxonomy	Tests
Marks	**50**
Remember	10
Understand	10
Apply	20
Analyze	10
Evaluate	-
Create	-