NEW HORIZON
COLLEGE OF ENGINEERING

A
Report on

" FACULTY DEVELOPMENT PROGRAM
on
DIGITAL SYSREM DESIGN USING INTEL FPGAs"

REGISTRATION FORM

Five Days Faculty Development Program on

"Digital System Design using Intel FPGAs"

September 26th – 30th 2022

1. Name: _____
2. Title/Position: _____
3. Organization: _____
4. Contact Address: _____
5. Email: _____
6. Phone(s): _____
7. Areas of Interest: _____

Applicant's Signature

Chief Patron
Dr. Mohan Manghnani
Chairman,
New Horizon Educational Institution, Bengaluru

Patron
Dr. Manjunatha
Principal
New Horizon College of Engineering, Bengaluru

Conveners
Dr. Sanjeev Sharma
Dean - QASDC
New Horizon College of Engineering, Bengaluru.

Dr. R J Anandhi
Dean-Academics
New Horizon College of Engineering, Bengaluru.

Organizing Coordinators:
Dr. G. Rajesh
Associate Professor, ECE

Dr. A. B. Gurulakshmi
Associate Professor, ECE

NEW HORIZON
COLLEGE OF ENGINEERING

Quality Assurance and Skill Development Center

In collaboration with

intel

Organizes

Five Days Faculty Development Program

On

"Digital System Design using Intel FPGAs"

September 26th –30th 2022

VLSI Lab, Chhatrapati Shivaji Block

DETAILED REPORT

Date(s) of Conduction : 26th to 30th September 2022

Venue : VLSI Lab, Chhatrapati Shivaji Block, NHCE

PROGRAM SCHEDULE

Resource Person : Mr. Padmanaban, Intel Corporation, Bangalore.

Profile

Padmanaban K

- Padmanaban is the Software Enabling and Optimization Engineer in Customer Experience Group at Intel PSG.
- Padmanaban has a post graduate degree in Applied Electronics from Anna University, Chennai and Bachelors in EEE from GCT, Coimbatore.
- He has 15+ years of experience in digital design for both FPGA and ASIC.
- Prior to joining Intel, he worked as a Chief Faculty in Sandeepani School of VLSI design (Training division of CoreEL Technologies, Bangalore) and as an Assistant Professor and Project Coordinator in MSRSAS, Bangalore

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Day	Date	Time: 9:30 a.m. to 12:30 p.m.	Time: 1:45 p.m. to 4:30 p.m.
1	26.09.2022	Introduction to Intel FPGAs and Quartus Tool Flow	FPGA design and implementation - Virtual labs with remote console
2	27.09.2022	Introduction to Timing Analysis - Applying Timing Constraints	Timing Exceptions - False Paths and Multicycle Paths - Achieving timing closure- Hands on Lab
3	28.09.2022	Introduction to Intel SoC FPGAs - IP design and Platform designer	SoC Design Flow- Basic SoC lab demo with hands on
4	29.09.2022	High Level Design using Intel FPGAs	HLS Implementation with hands on Lab
5	30.09.2022	Introduction to FPGA Memory - Internal and External	Single Port and Dual Port RAM - Design Flow for an External SDRAM

Department of Quality Assurance and Skill Development Center in collaboration with Intel Corporation has organized **Faculty Development Program** for Faculty members of ECE, CSE, ISE, and EEE from 26th to 30th September 2022. This FDP is focused on exposing participants to latest tools related to digital system design for applications using FPGA and SoC FPGAs. The participants will gain a better understanding of utilizing FPGA based control techniques to solve engineering challenges. Day 1 started by felicitating the resource person Mr. Padmanaban, Software Enabling and Optimization Engineer - CEG - Intel PSG by Dr. Sanjeev Sharma, Dean – QASDC.

Figure 1 Felicitation to Resource Person by Dean QASDC

Figure 2 Dr. Sanjeev Sharma, Dean QASDC addressing the program

Day 1: 26th Sept. 2022

The first session began with an introduction to Intel FPGAs and the Quartus Tool Flow; types of Intel FPGAs; simulation synthesis; analysis and elaboration; analysis and synthesis; fitter and programming file production.

Session 2 of day 1 was completely on design and implementation of FPGA in virtual labs with a remote console, are given. For examples of verilog FULL ADDER and SWITCH TO LED, the participants validated the output on the DE10 LITE board in LABSLAND.

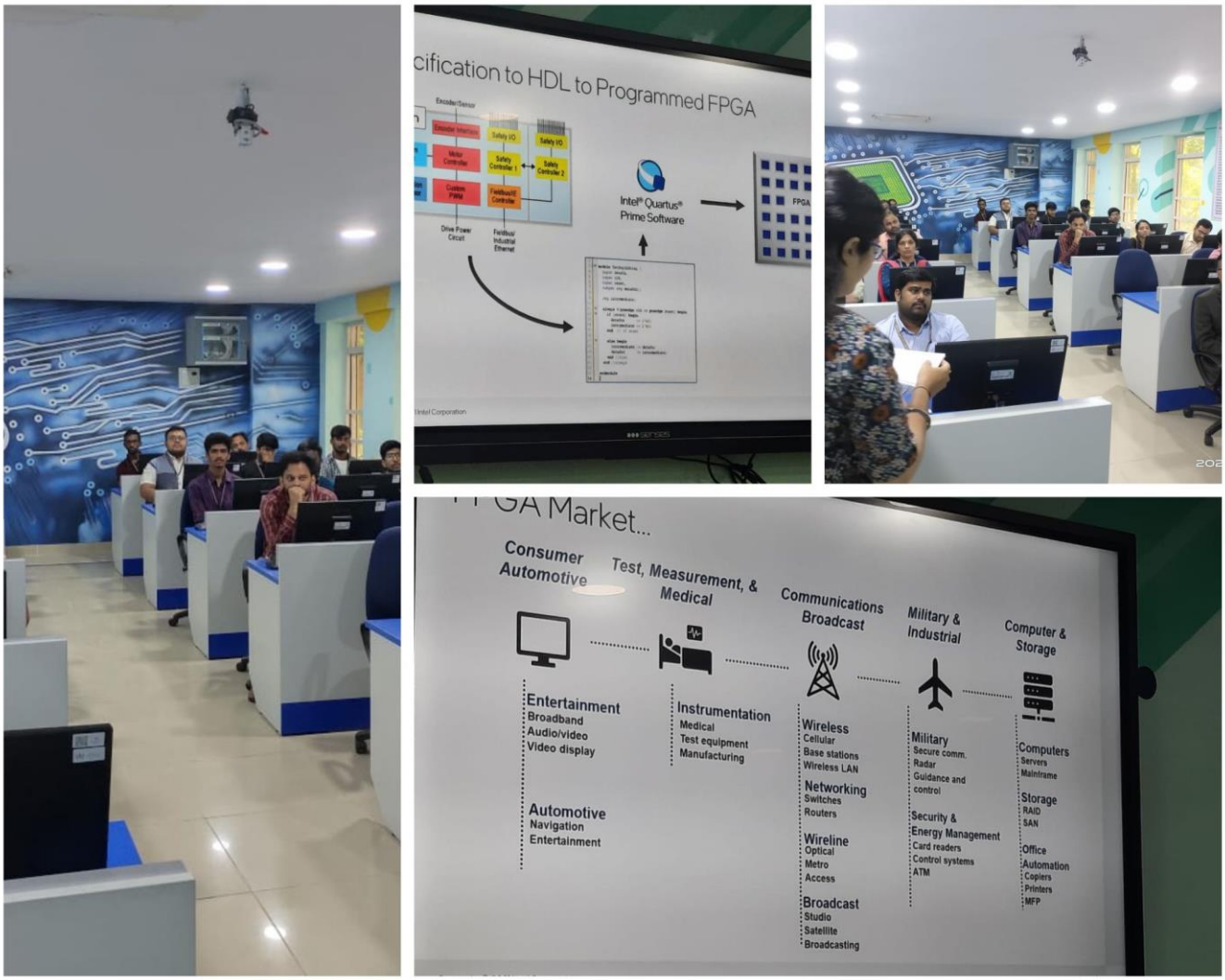


Figure 3 Day 1 Glimpses

Day 2: 27th Sept. 2022

The second day began with an introduction to timing analysis and the application of timing constraints to FPGAs. The following topics are covered: adding pin restrictions; timing constraints by establishing a clock; setting maximum and minimum delay; producing the SDC file; and adding it to the QUARTUS project. Timing Exceptions-False Paths and Multi-Cycle Paths -Achieving Timing Closure-Hands-on Lab for several quartus project files were covered in session 2 of day 2.

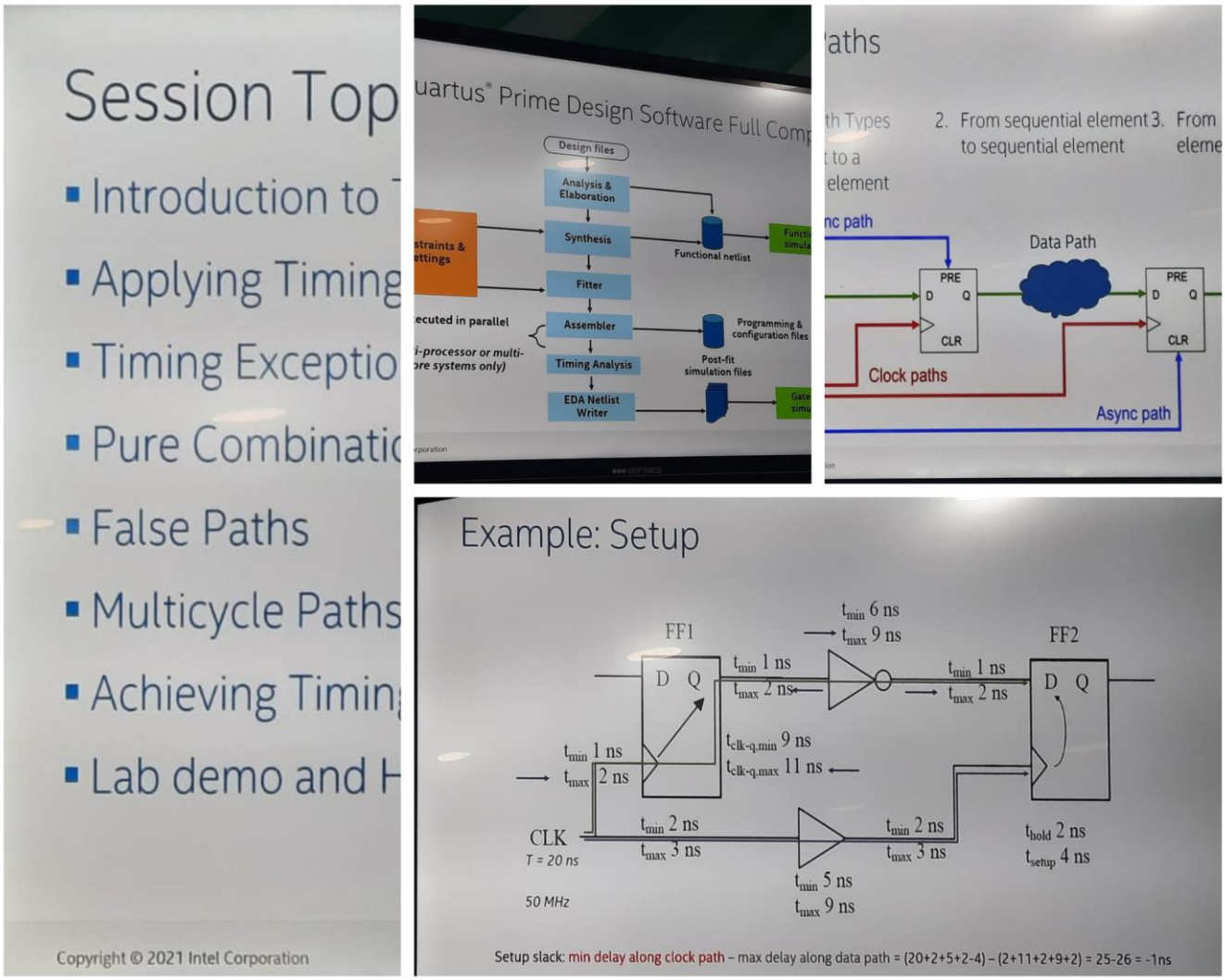


Figure 4 Day 2 Glimpses

Day 3: 28th Sept. 2022

The third day was all about Intel SoCs. The resource person investigated the IP design and platform designer for Intel SoC-Adding of IP cores available from the platform designer to develop a project, including the CPU or on-chip memory, UART JTAG, switch, button, and hex display to produce a complete SYSTEM ON CHIP. The practical session addressed SoC Design Flow-Basic SoC lab demo with a hands-on lab for the constructed SOC and its area, power, and timing analyses.

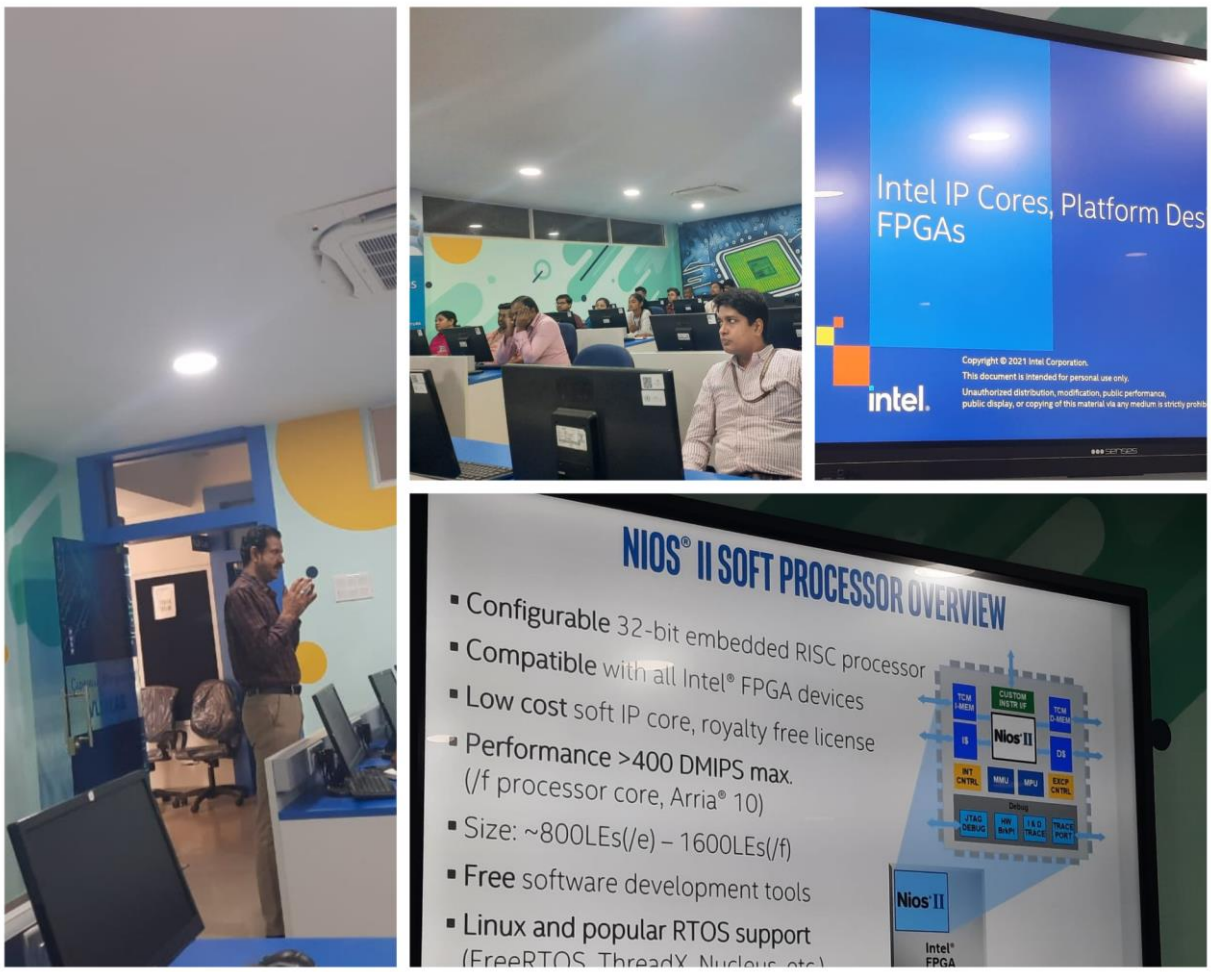


Figure 5 Day 3 Glimpses

Day 4: 29th Sept. 2022

Day 4's morning session is entirely dedicated to completing the assignments in the style of a mini HACKATHON. Later, the High Level Design employing Intel FPGAs and their requirement and utilisation of high level synthesis, commands for HLS, development of a c, c++ code, and comparison of HLS and HDL will be covered.

HLS implementation with hands-on lab is accomplished by the synthesis of an HLS project, a Verilog project, and an IP project, as well as a comparison of performance in terms of area and power.

Figure 6 Day 4 Sessions

Day 5: 30th Sept. 2022

The final day started with an exploration of the memory used in FPGAs. FPGA Memory Overview-Internal and External: On-chip vs. external memory on board, pros and cons. Single Port and Dual Port RAM-External SDRAM Implementation of various projects created on the DE10 LITE Intel FPGA. An overview of Intel FPGAs and applications

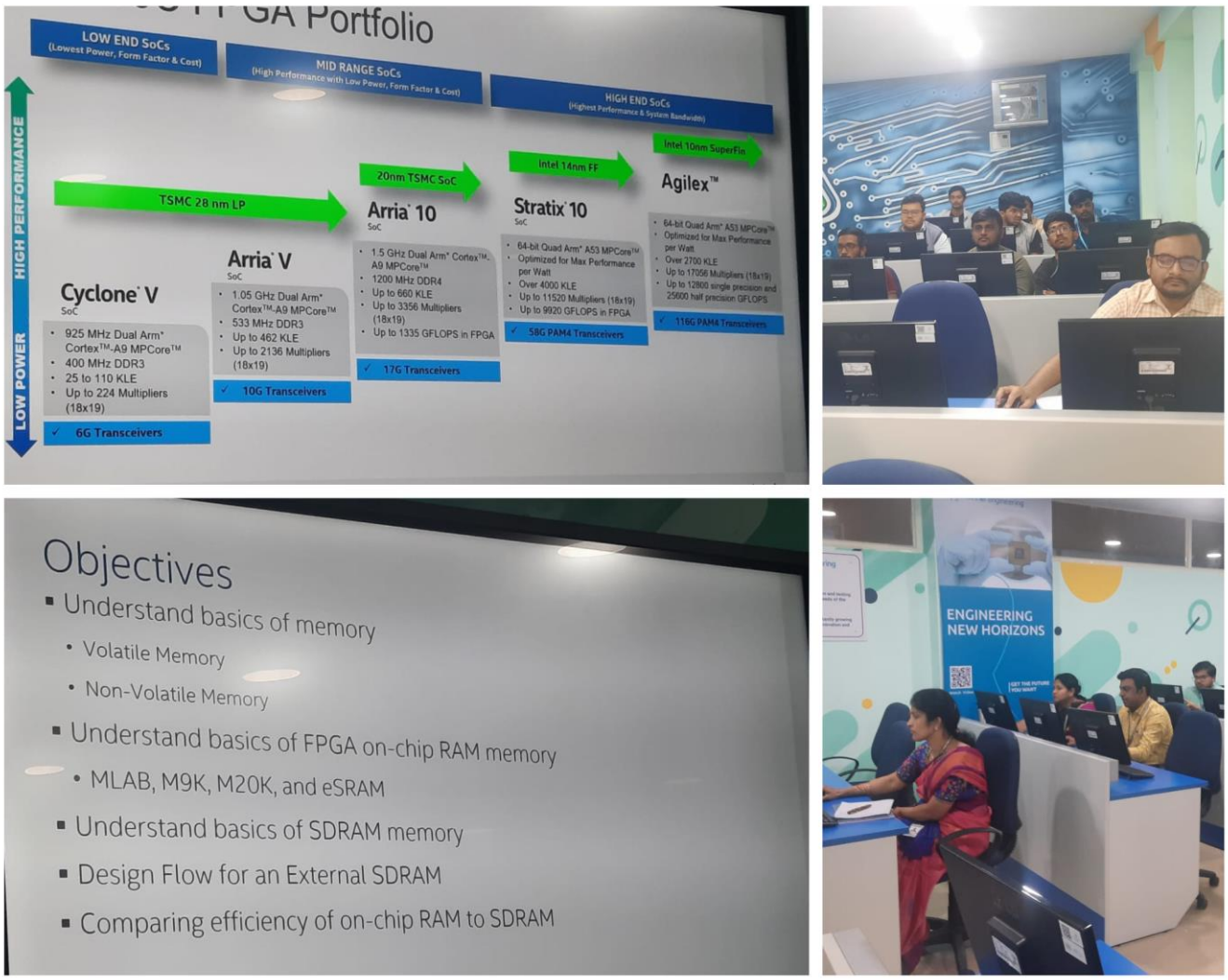
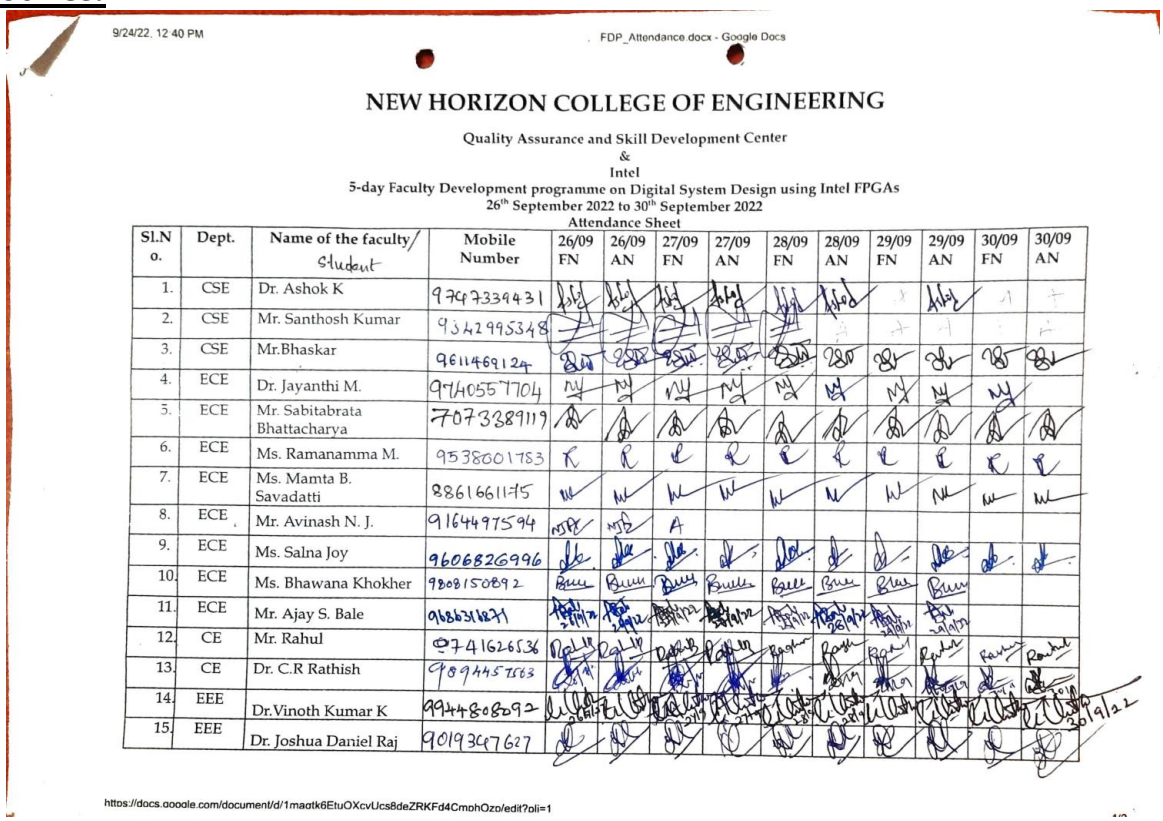


Figure 7 Glimpses of Day 5

Attendance:



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NEW HORIZON COLLEGE OF ENGINEERING

Quality Assurance and Skill Development Center
&
Intel
5-day Faculty Development programme on Digital System Design using Intel FPGAs
26th September 2022 to 30th September 2022
Attendance Sheet

Sl.No.	Dept.	Name of the faculty/ Student	Mobile Number	26/09 FN	26/09 AN	27/09 FN	27/09 AN	28/09 FN	28/09 AN	29/09 FN	29/09 AN	30/09 FN	30/09 AN
1.	CSE	Dr. Ashok K	9747339431										
2.	CSE	Mr. Santhosh Kumar	9342995348										
3.	CSE	Mr.Bhaskar	9611469124										
4.	ECE	Dr. Jayanthi M.	9740557704										
5.	ECE	Mr. Sabitabrata Bhattacharya	7073389119										
6.	ECE	Ms. Ramanamma M.	9538001783										
7.	ECE	Ms. Mamta B. Savadatti	8861661175										
8.	ECE	Mr. Avinash N. J.	9164497594										
9.	ECE	Ms. Salna Joy	9606826996										
10.	ECE	Ms. Bhawana Khokher	9808150892										
11.	ECE	Mr. Ajay S. Bale	9686318271										
12.	CE	Mr. Rahul	9741626536										
13.	CE	Dr. C.R Rathish	9894457563										
14.	EEE	Dr.Vinoth Kumar K	9944808092										
15.	EEE	Dr. Joshua Daniel Raj	9019367627										

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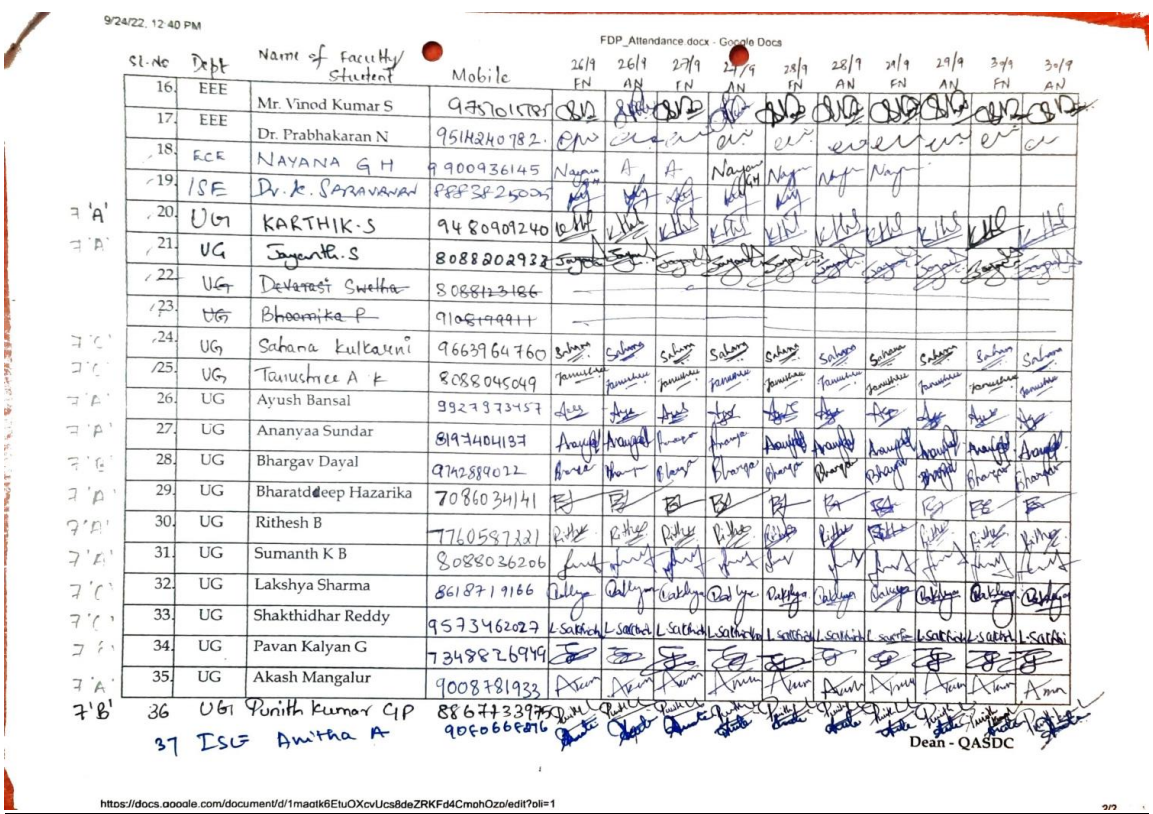

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Sl.No	Dept	Name of Faculty/ Student	Mobile	26/9 FN	26/9 AN	27/9 FN	27/9 AN	28/9 FN	28/9 AN	29/9 FN	29/9 AN	30/9 FN	30/9 AN
16.	EEE	Mr. Vinod Kumar S	9751015787										
17.	EEE	Dr. Prabhakaran N	9514240782										
18.	ECE	NAYANA G H	9900936145										
19.	ISE	Dr. K. SARAVANAN	8884825025										
20.	UG	KARTHIK.S	9480909240										
21.	UG	Jayanth.S	8088202932										
22.	UG	Devaraj Swetha	8088123186										
23.	UG	Bhoomika P	9108199911										
24.	UG	Sahana Kulkarni	9663964760										
25.	UG	Tanushree A K	8088045049										
26.	UG	Ayush Bansal	9929973457										
27.	UG	Ananyaa Sundar	8197404137										
28.	UG	Bhargav Dayal	9742889022										
29.	UG	Bharatdeep Hazarika	7086034141										
30.	UG	Rithesh B	7760587221										
31.	UG	Sumanth K B	8088036206										
32.	UG	Lakshya Sharma	8618719166										
33.	UG	Shakthidhar Reddy	9573462027										
34.	UG	Pavan Kalyan G	7348826949										
35.	UG	Akash Mangalur	9008781933										
36	UG	Punith Kumar CP	8867733975										
37	ISE	Anitha A	9066668876										

Dean - QASDC

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Feedback:

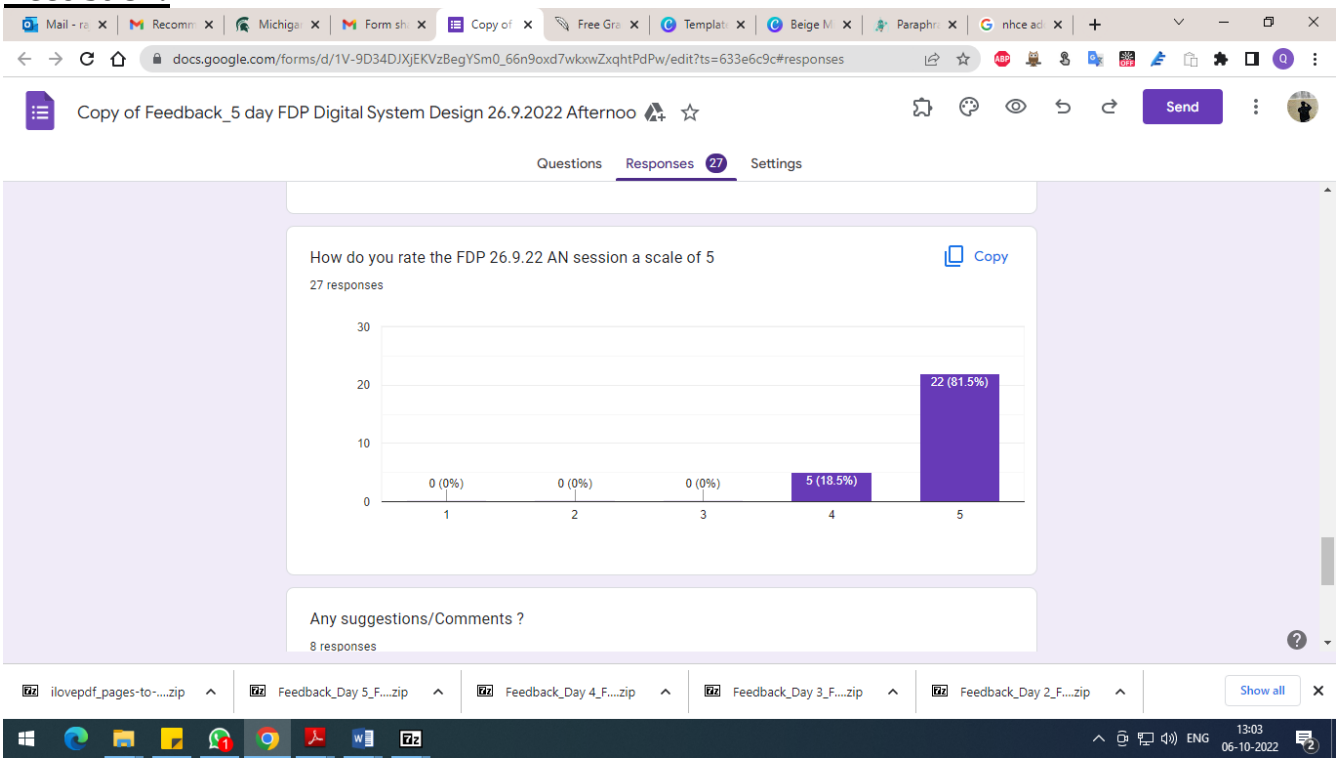

Figure 8 Day 1 session feedback

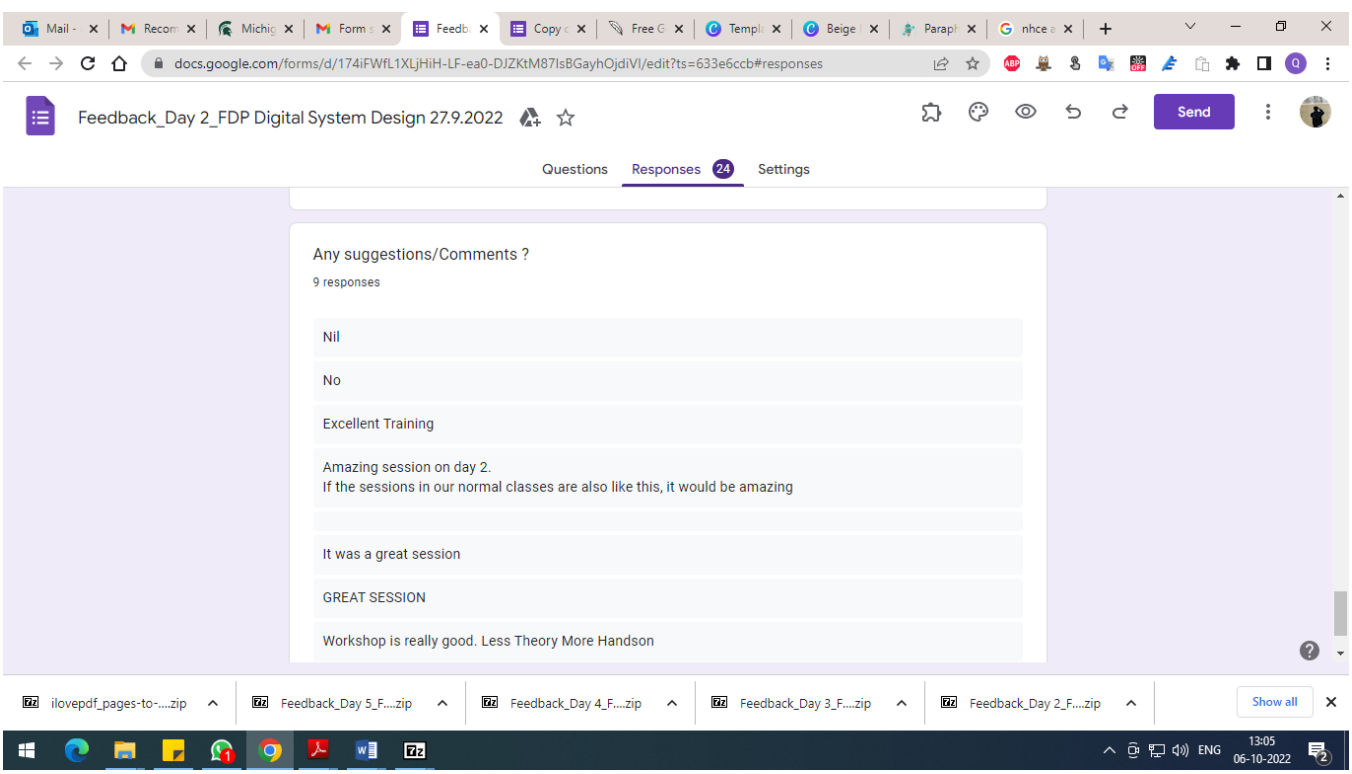

Figure 9 Day 2 Feedback

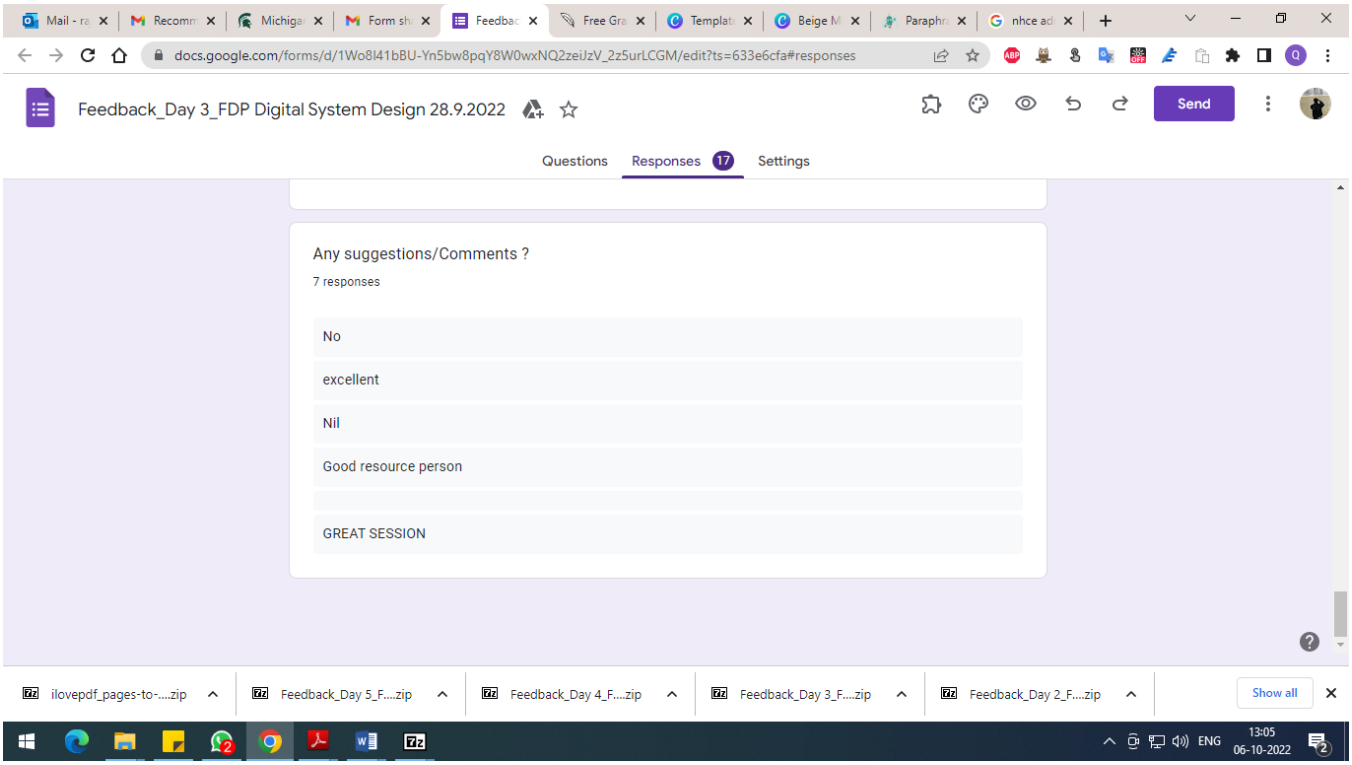

Figure 10 Day 3 Session's Feedback

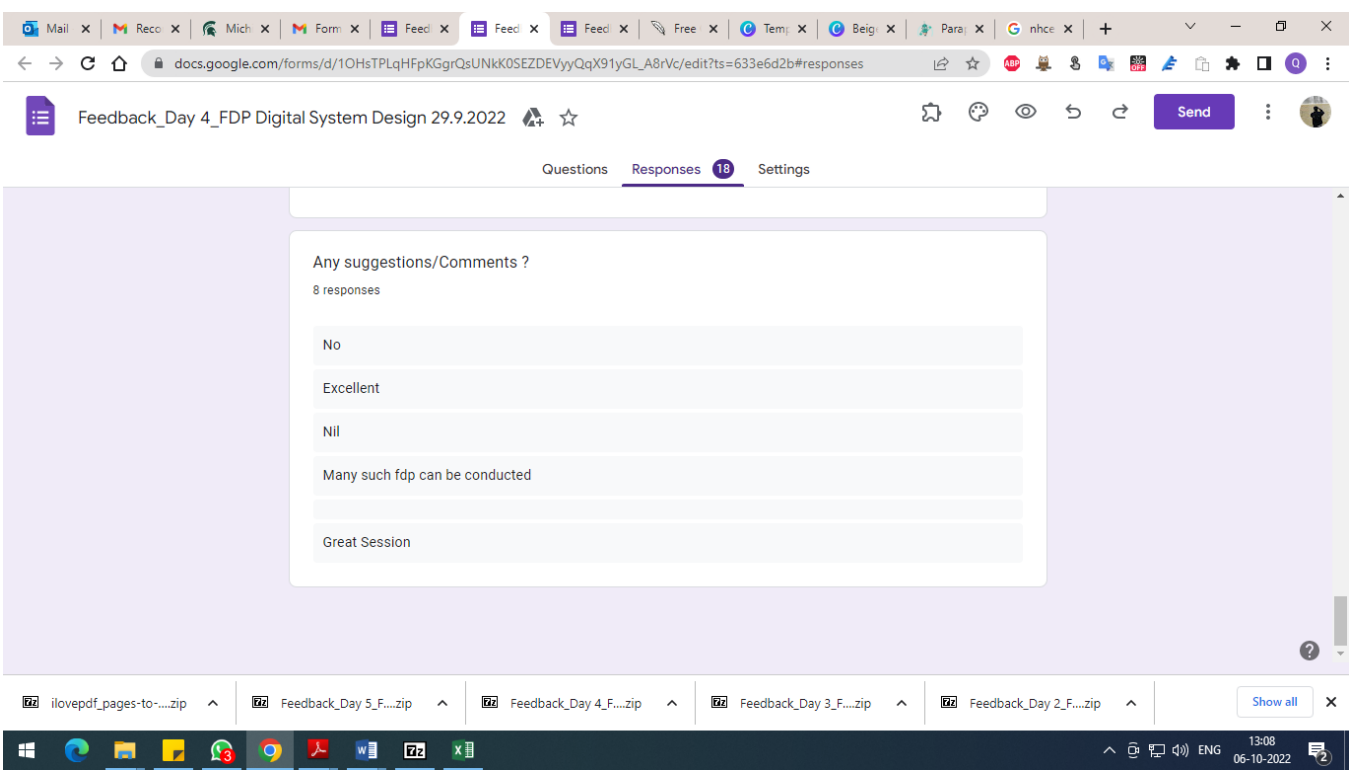

Figure 11 Day 4 Session's Feedback

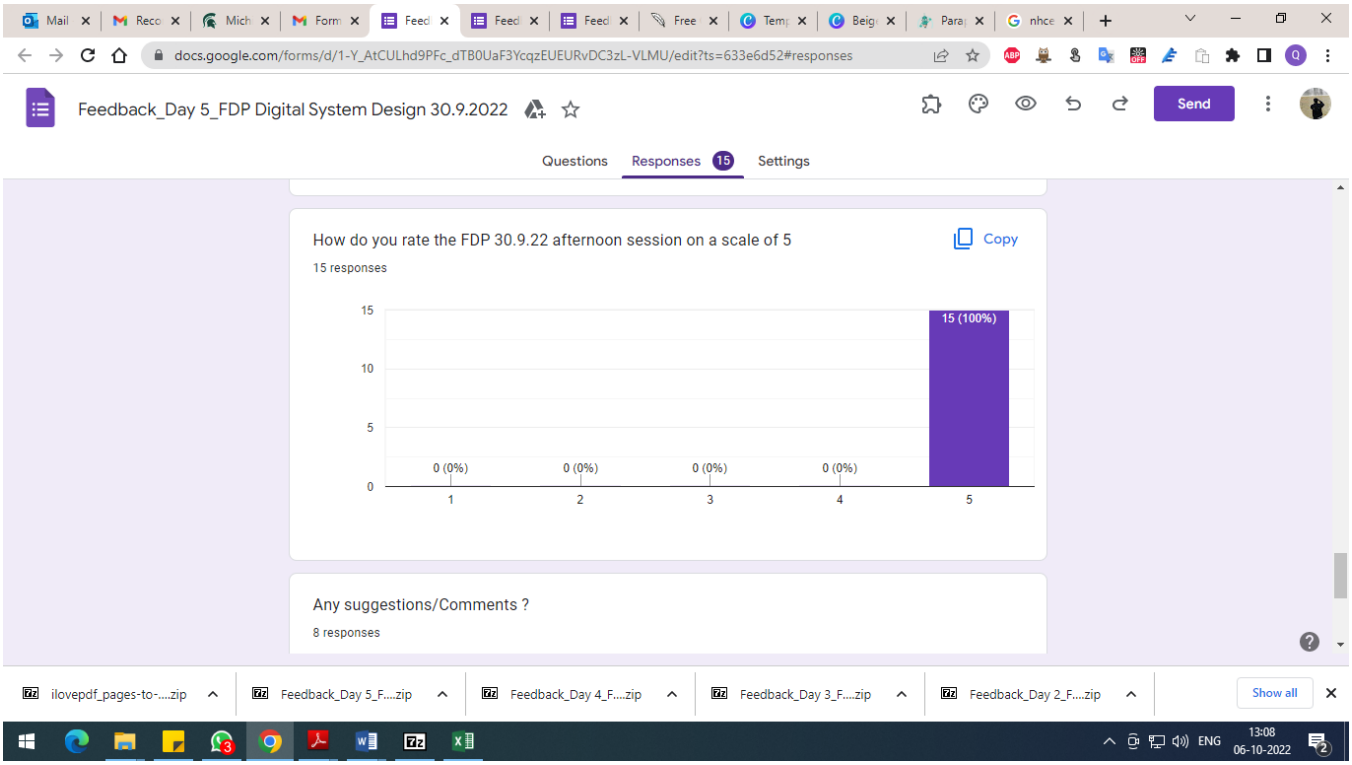

Figure 12 Overall Feedback

Summary of Feedback:

- ✓ Amazing sessions.
- ✓ If the sessions in our normal classes are also like this, it would be amazing
- ✓ It was a great session
- ✓ GREAT SESSION
- ✓ Workshop is really good. Less Theory More Handson.
- ✓ Good resource person
- ✓ Many such FDP/Trainings can be conducted

Key Outcomes:

- ➢ Participants were be able to apply the experience gained from FDP to strengthen the core engineering skills using the hardware FPGA kits & Intel Quartus Prime design software.
- ➢ Looking forward to include Quartus in the curriculum to enrich the students in design and analysis using FPGA kits.