

## A Report on

# "FACULTY DEVELOPMENT PROGRAM on DIGITAL SYSREM DESIGN USING INTEL FPGAs"

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Five Days Faculty Development Program on "Digital System Design using Intel FPGAs" September 26<sup>th</sup> – 30<sup>th</sup> 2022

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7. Areas of Interest: \_\_\_\_

Chief Patron Dr. Mohan Manghnani Chairman, New Horizon Educational Institution, Bengaluru

Patron

**Dr. Manjunatha** Principal New Horizon College of Engineering, Bengaluru

Conveners Dr. Sanjeev Sharma Dean - QASDC New Horizon College of Engineering, Bengaluru.

**Dr. R J Anandhi** Dean-Academics New Horizon College of Engineering, Bengaluru.

Organizing Coordinators: Dr. G. Rajesh Associate Professor, ECE

Dr. A. B. Gurulakshmi Associate Professor, ECE



Quality Assurance and Skill Development Center

In collaboration with

intel

Organizes

Five Days Faculty Development Program
On



Applicant's Signature

## **DETAILED REPORT**

Date(s) of Conduction

: 26<sup>th</sup> to 30<sup>th</sup> September 2022

Venue

: VLSI Lab, Chhatrapati Shivaji Block, NHCE

#### **PROGRAM SCHEDULE**

Resource Person : Mr. Padmanaban, Intel Corporation, Bangalore.

Profile

### Padmanaban K



- Padmanaban is the Software Enabling and Optimization Engineer in Customer Experience Group at Intel PSG.
- Padmanaban has a post graduate degree in Applied Electronics from Anna University, Chennai and Bachelors in EEE from GCT, Coimbatore.
- He has 15+ years of experience in digital design for both FPGA and ASIC.
- Prior to joining Intel, he worked as a Chief Faculty in Sandeepani School of VLSI design (Training division of CoreEL Technologies, Bangalore) and as an Assistant Professor and Project Coordinator in MSRSAS, Bangalore

Day	Date	Time: 9:30 a.m. to 12:30 p.m.	Time: 1:45 p.m. to 4:30 p.m.
1	26.09.2022	Introduction to Intel FPGAs and Quartus Tool Flow	FPGA design and implementation - Virtual labs with remote console
2	27.09.2022	Introduction to Timing Analysis - Applying Timing Constraints	Timing Exceptions - False Paths and Multicycle Paths - Achieving timing closure- Hands on Lab
3	28.09.2022	Introduction to Intel SoC FPGAs - IP design and Platform designer	SoC Design Flow- Basic SoC lab demo with hands on
4	29.09.2022	High Level Design using Intel FPGAs	HLS Implementation with hands on Lab
5	30.09.2022	Introduction to FPGA Memory - Internal and External	Single Port and Dual Port RAM - Design Flow for an External SDRAM

Department of Quality Assurance and Skill Development Center in collaboration with Intel Corporation has organized **Faculty Development Program** for Faculty members of ECE, CSE, ISE, and EEE from 26<sup>th</sup> to 30<sup>th</sup> September 2022. This FDP is focused on exposing participants to latest tools related to digital system design for applications using FPGA and SoC FPGAs. The participants will gain a better understanding of utilizing FPGA based control techniques to solve engineering challenges. Day 1 started by felicitating the resource person Mr. Padmanaban, Software Enabling and Optimization Engineer - CEG - Intel PSG by Dr. Sanjeev Sharma, Dean – QASDC.



Figure 1 Felicitation to Resource Person by Dean QASDC



Figure 2 Dr. Sanjeev Sharma, Dean QASDC addressing the program

#### Day 1: 26<sup>th</sup> Sept. 2022

The first session began with an introduction to Intel FPGAs and the Quartus Tool Flow; types of Intel FPGAs; simulation synthesis; analysis and elaboration; analysis and synthesis; fitter and programming file production.

Session 2 of day 1 was completely on design and implementation of FPGA in virtual labs with a remote console, are given. For examples of verilog FULL ADDER and SWITCH TO LED, the participants validated the output on the DE10 LITE board in LABSLAND.





Day 2: 27<sup>th</sup> Sept. 2022

The second day began with an introduction to timing analysis and the application of timing constraints to FPGAs. The following topics are covered: adding pin restrictions; timing constraints by establishing a clock; setting maximum and minimum delay; producing the SDC file; and adding it to the QUARTUS project. Timing Exceptions-False Paths and Multi-Cycle Paths -Achieving Timing Closure-Hands-on Lab for several quartus project files were covered in session 2 of day 2.





#### Day 3: 28<sup>th</sup> Sept. 2022

The third day was all about Intel SoCs. The resource person investigated the IP design and platform designer for Intel SoC-Adding of IP cores available from the platform designer to develop a project, including the CPU or on-chip memory, UART JTAG, switch, button, and hex display to produce a complete SYSTEM ON CHIP. The practical session addressed SoC Design Flow-Basic SoC lab demo with a hands-on lab for the constructed SOC and its area, power, and timing analyses.



Figure 5 Day 3 Glimpses

Day 4: 29th Sept. 2022

Day 4's morning session is entirely dedicated to completing the assignments in the style of a mini HACKATHON. Later, the High Level Design employing Intel FPGAs and their requirement and utilisation of high level synthesis, commands for HLS, development of a c, c++ code, and comparison of HLS and HDL will be covered.

HLS implementation with hands-on lab is accomplished by the synthesis of an HLS project, a Verilog project, and an IP project, as well as a comparison of performance in terms of area and power.



Figure 6 Day 4 Sessions

#### Day 5: 30<sup>th</sup> Sept. 2022

The final day started with an exploration of the memory used in FPGAs. FPGA Memory Overview-Internal and External: On-chip vs. external memory on board, pros and cons. Single Port and Dual Port RAM-External SDRAM Implementation of various projects created on the DE10 LITE Intel FPGA. An overview of Intel FPGAs and applications





# Objectives

- Understand basics of memory
  - Volatile Memory
  - Non-Volatile Memory
- Understand basics of FPGA on-chip RAM memory
- MLAB, M9K, M20K, and eSRAM
- Understand basics of SDRAM memory
- Design Flow for an External SDRAM
- Comparing efficiency of on-chip RAM to SDRAM



Figure 7 Glimpses of Day 5

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Figure 12 Overall Feedback

#### **Summary of Feedback:**

- ✓ Amazing sessions.
- $\checkmark$  If the sessions in our normal classes are also like this, it would be amazing
- $\checkmark$  It was a great session
- ✓ GREAT SESSION
- ✓ Workshop is really good. Less Theory More Handson.
- $\checkmark$  Good resource person
- ✓ Many such FDP/Trainings can be conducted

#### **Key Outcomes:**

- Participants were be able to apply the experience gained from FDP to strengthen the core engineering skills using the hardware FPGA kits & Intel Quartus Prime design software.
- Looking forward to include Quartus in the curriculum to enrich the students in design and analysis using FPGA kits.