

Department of Electronics and Communication Engineering

13.04.2018

## EXPERT LECTURE

The ECE students are hereby informed that Expert Lecture is scheduled on

"FPGA Implementation"

on 16.04.2018

By

## Mr Shashikanth Patil

Senior Project Engineer, Wipro Technologies Ltd, Bangalore

Timing schedule is as follows

Sl. No	Timings	Semester
1	9:30AM-11:30AM	4 <sup>th</sup> (A, B&C)

Respective subject teachers are hereby informed to be present in the Seminar Hall during the schedule.

Note: All Faculty members are invited to attend the same (without affecting regular classes)

Venue: Falconary Seminar Hall

Varyhir

Expert Lecture Faculty In-charge

#### Shashikanth Patil

#634, 2<sup>nd</sup> Floor, 7<sup>th</sup> Mainroad, Vijayanagar, Bengaluru – 560040 Email ID: shashi.vnit@gmail.com; Contact: +91-9880962096

#### Career Objective:

To work in an innovative, challenging environment & help organization to achieve its objective in the most efficient manner by applying my skills, abilities and thereby growing with the organization.

#### **Profile Summary:**

- 7.5+ years of experience in FPGA/ASIC Design, RTL Simulation, Synthesis, Creating testbench environment & Verification. Additional 2.2+ years of experience in Training & Academics.
- Experience in IP/Block Level Verification with Constraint Random, Assertions & Functional Coverage; creating verification environment with SystemVerilog, Verilog/VHDL & UVM/OVM.
- Experience with EDA Tools such as Synopsys VCSMX, Verdi/ DVE; QuestaSim v10.1c, Xilinx ISE v12.1 and FPGA Spartan 3E, Virtex 5; Programming & Scripting witsh MATLAB, C & Perl.
- Working knowledge on Peripheral Interface & OnChip Protocols AMBA AXI/AHB, OCP, SPI, UART & USB 3.x, and complete Wind-Profiler Radar Sub-Systems.
- Work experience on Lab Equipments/Diagnostic tools such as Signal Generator, Oscilloscope, Spectrum Analyzer and Network Analyzer.

#### Professional Experience:

WIPRO Technologies Ltd., Bengaluru
 Designation: Senior Project Engineer

Duration: Jan 2015 to till date

Spanwave Technology Solutions Pvt. Ltd., Bengaluru Designation: Senior Engineer

Duration: July 2010 to Dec 2014

New Horizon College of Engineering., Bengaluru Designation: Teaching Staff (Lecturer)

Duration: Feb 2009 to May 2010

C2C Semiconductors Pvt. Ltd., Bengaluru
 Designation: Member Technical Staff

Duration: April 2008 to Jan 2009

#### **Education Qualification:**

- M.Tech (Embedded Electronic Systems) from Visvesvaraya National Institute of Technology (NIT/REC), Nagpur (Maharastra, INDIA) during 2005 07.
- B.E. (Electronics & Communication Engineering) from Visvesvaraya Technological University, Belgaum (Karnataka, INDIA) during 2001 – 05.

Achievement: Qualified GATE - 2005 with 97.5 percentile (All India Rank - 915)

I hereby declare that the above particulars are true and correct to the best of my knowledge.

SHASHIKANTH PATIL

# Expert Le Chure (Syrlem Destron using Hor)

## NEW HORIZON COLLEGE OF ENGINEERING DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING IV Sem "A" Sec

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For highlighted students, attendance should not be called in any of the classes until the

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79	INH17EC431	VASANTH.R	Rakosh

Note:

For highlighted students, attendance should not be called in any of the classes



Sachin V <sachuv91@gmail.com>

### Regarding expert lecture

3 messages

Sachin V <sachuv91@gmail.com>

To: shashi.vnit@gmail.com

Wed, Apr 11, 2018 at 5:37 PM

Cc: Aravinda Koithyar <aravindake@gmail.com>, karthikvishwanath1990 <karthikvishwanath1990@gmail.com>

Hi sir.

As discussed, we have scheduled the expert lecture for system design using HDL on Monday at 9:30. We require your official confirmation through mail and following details for initiating remuneration process.

Details required : Pan no , aadhar , date of birth, bank name account no, ifsc code and branch

Regards, Sachin V

hashikanth Patil <shashi.vnit@gmail.com> To: Sachin V <sachuv91@gmall.com>

Thu, Apr 12, 2018 at 5:45 PM

Cc: Aravinda Koithyar <aravindake@gmail.com>, karthikvishwanath1990 <karthikvishwanath1990@gmail.com>

Hi Sir.

Thank you for the opportunity, will be available for Guest Lecture on April 16, 2018 as per the schedule.

Pls find the required information below:

PAN Details:

Date of Birth: April 05, 1984

Bank Details:

Bank Name: State Bank of India

A/C No. · CHARLES AND A IFSC Code: SBIN0003023

: Rajaji Nagar 5th Block, Bengaluru Branch

Thanks & Regards,

Shashikanth Patil

[Quoted text hidden]

Shashikanth Patil <shashi.vnit@gmail.com>

Tue, Apr 17, 2018 at 1:22 PM

To: Sachin V <sachuv91@gmail.com>

Cc: Aravinda Koithyar <aravindake@gmail.com>, karthikvishwanath1990 <karthikvishwanath1990@gmail.com>

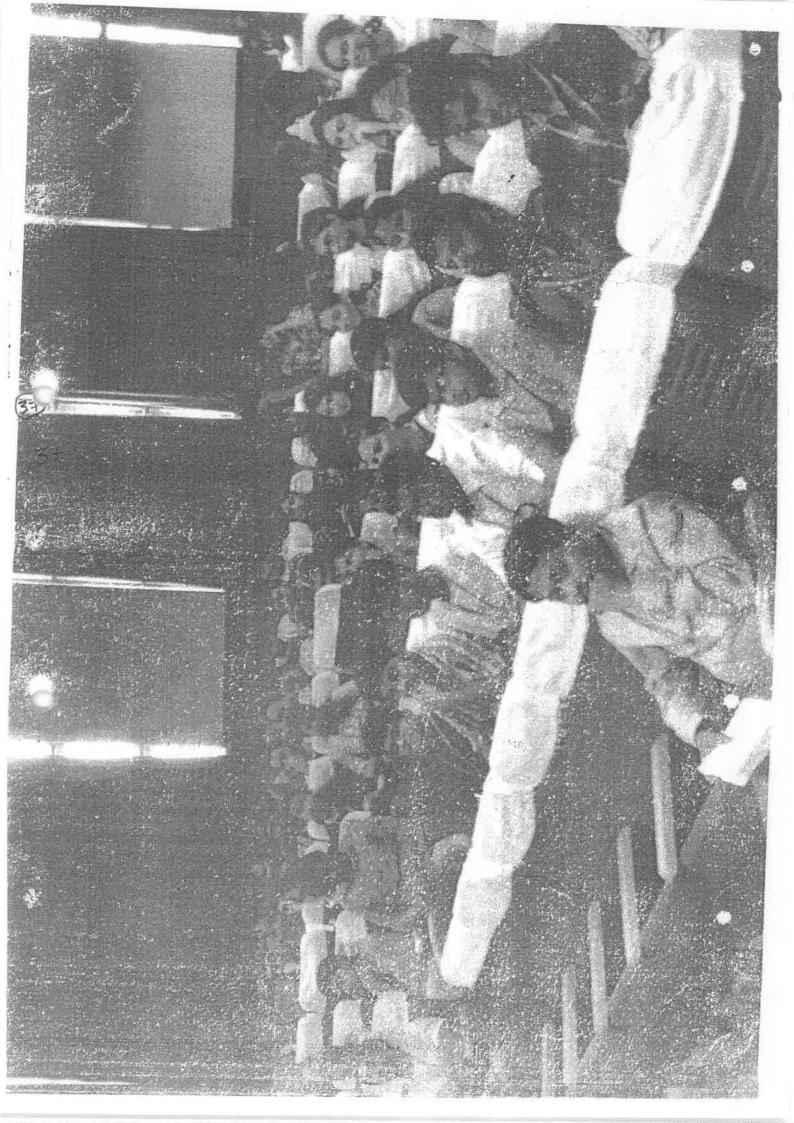
Hello Sir.

Pls find the attached Guest Lecture PPTs " VLSI"- Digital System Design, Validation & Career Opportunities".

Thanks & Regards,

Shashikanth Patil

[Quoted text inidden]



#### **REPORT ON GUEST LECTURE**

#### **SHASHIKANT PATIL**

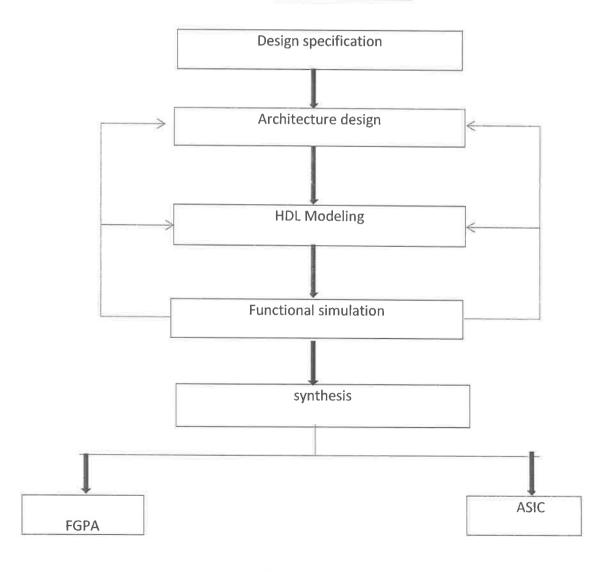
**NAME: GURURAJ NATIKAR** 

USN:1NH17EC407 4<sup>th</sup> sem 'B'section

**SUB:HDL** 

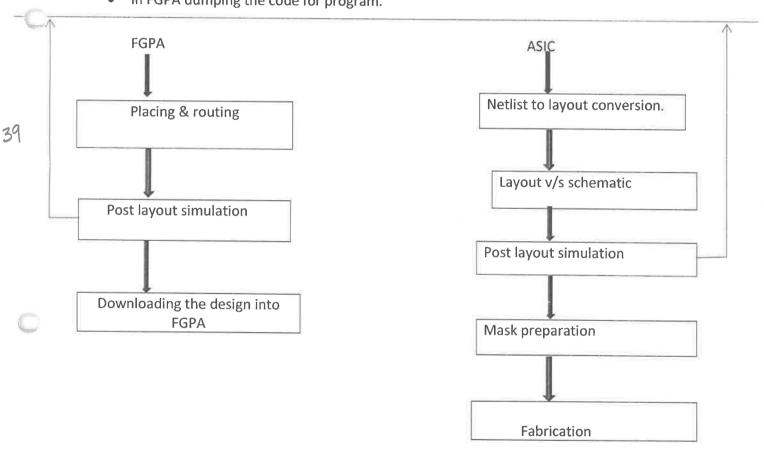
- Moore's prediction
- Intel is planning to launch 10nm.

#### VLSI IC DESIGN FLOW



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- Go & implement.
- Called state machine & finite state machine.
- These are all design specification.
- Example is traffic light controller.
- Architecture design is to implement the traffic light controller.
- Simulation is to simulate the program.
- Synthesis block it take to the input of the functional simulation.
- It generate the program.
- There are 2domains ie 1)FGPA 2)ASIC
- ASIC(Application specific integrated circuit).
- In FGPA dumping the code for program.



**FGPA** 

**ASIC** 

- These are in built steps.
- Mask preparation & fabrication is done by fabrication block.

#### ASIC s V/S FGPAs

Depends on cost, total availability, performance & design flexibility.

#### Field programmable gate arrays(FGPAs)

- Faster time to market.
- No non recurring expenses (NRE).
- Simpler design cycle.field programmability & reusability.
- Good for prototyping & limited production.
- But
- Power consumption is more.(this is where as ASIC wins the race.)
- You have to use resources available in FGPA.
- Used for lower speed, lower complexity & lower volume designs.

#### Application for specific integrated circuits(ASICs)

- Cost...cost....lower unit cost.
- ASICs faster than FGPA.
- Low power consumption.
- You can implement analog/mixed signal design circuits which is not possible in FGPA.

#### Major market segments for FGPAs

- Digital signal processing.
- Embedded microcontroller.
- Aerospace, defense space communication technology.
- Physical layer communication.

#### FGPAs programming techniques

- Antifuse based devices.
- SRAM based devices.
- FLASH EPROM based devices.
- Hybrid FLASH-SRAM based devices.

#### Overview on HDLs(VHDL/Verilog)

- HDL is a software programming language used to model the intended operation of a piece of hardware.
- The developments of VHDL begin in 1983 by US. Department of defence &in 1987 it was adopted as IEEE.standard 1076.
- In 1983 gateway design automation released Verilog HDL.
- Two basic constructs of procedural assignments are initial& always block.

#### Blocking & non-blocking assignments

blocking non-blocking
ex:reg[1:0]reg\_a,reg\_b; ex:reg[1:0]reg\_a,reg\_b;
intial intial
begin begin
reg\_a=#10 2'b10; reg\_b=#5 2'b01;
reg\_b=#5 2'b01; reg\_b<=#5 2'b01;

Equal symbol is used'='

symbol is used '<='.

#### Parameter's/define

Parameters are used to specify constants.

#### Finite state machines(FSMS)

State are4.

AI

- Using 4flipflops.
- Synchronous & asynchronous reset.
- Verification role in IC design.
- Front-End VLSI(deals with RTL coding).
- Back-End VLSI(deals with circuit/physical design).

Joulen V.