## NEW HORIZON COLLEGE OF ENGINEERING

### DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

08/02/2019

#### **GUEST LECTURE**

This is to inform to IV semester students of ECE that the guest lecture is arranged on 9/02/19 at Falconary Seminar Hall between 2.50PM to 4.50PM.

Topic to be delivered: "VLSI - Transistor to Transformation"

Name of the Speaker: Mr.Shriram S

Designation : Hardware Design Engineer

Company : Intel Technologies, Bangalore

Respective subject teachers are hereby informed to be present at Falconary Seminar Hall during the lecture.

All the faculty members are invited to attend the same without affecting the regular classes.

M. Dharmanh 8/2/19
Guest Lecture Coordinator

HOD-ECE

From the desk of:

Prof & HOD - Department of Electronics and Communication Engineering

02-01-2019

To, The Principal, NHCE NHCE/ECE/LTR/001/2019

Dear Sir,

Sub: Request for Falconry Hall on 9<sup>th</sup> February 2019, from 2.00pm to 4.00pm -reg

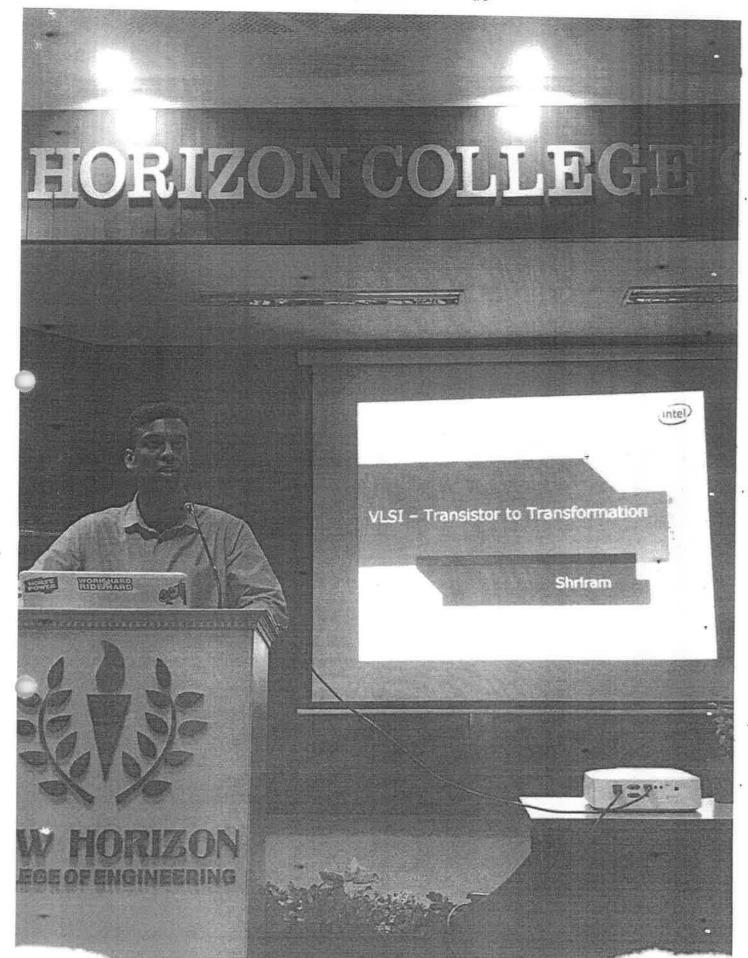
With reference to the above subject, guest lecture is scheduled on 9<sup>th</sup> February 2019 from 2.00pm to 4.00pm. I am hereby requesting you to permit us to use Falconry Seminar Hall on the above mentioned date and time.

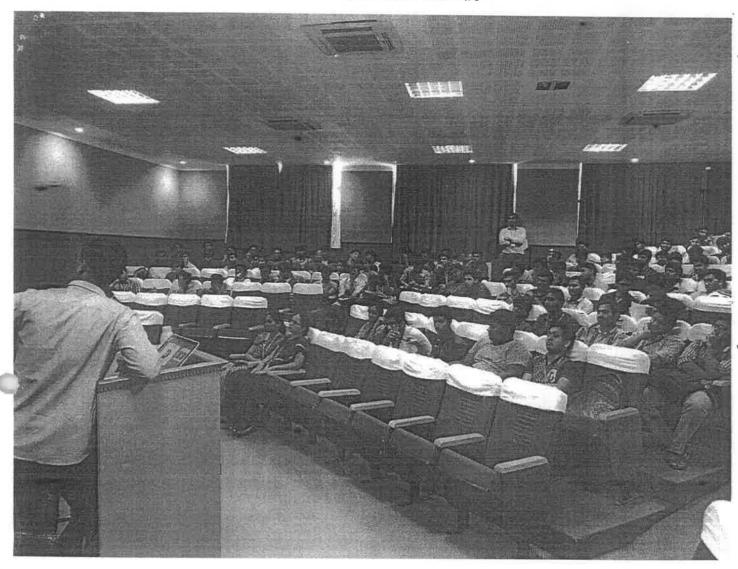
Thanking you

With Regards,

HOD-ECE

NEW HORIZON COLLEGE OF ENGINEERING





## NEW HORIZON COLLEGE OF ENGINEERING DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING IV Sem "B" Sec

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Note: Highlighted students should be informed to pay the Account dues. Students should not be given attendance till they clear the dues.

# NEW HORIZON COLLEGE OF ENGINEERING DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING IV Sem "C" Sec

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Note: Highlighted students should be informed to pay the Account dues. Students should not be given attendance till they clear the dues.

#### NEW HORIZON COLLEGE OF ENGINEERING DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING IV Sem "A" Sec

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Note: Highlighted students should be informed to pay the Account dues. Students should not be given attendance till they clear the dues.

NAME OF THE EVENT/CLUB: VLSI - FRANSISTOR TO TRANSFORMATION

FEEDBACK ON (Mention the topic): VLST - Treansistor 70 Transform DATE: 9/2/19 Instruction: Please put a tick mark at the appropriate column.

Clarity	Visuals	Skills	Guidonas	O 11
/			Guidance	Overall
	/	<b>V</b>	./	V
	•		•	
	Clarity	Clarity Visuals  /	Clarity Visuals Skills	Clarity Visuals Skills Guidance

Comments/Remarks/Suggestions:

1. The lecture was very informative and interesting we would like to have more of such audio-visual entrode in the future.

3.

Name & USN No.(optional)

NAME OF THE EVENT/CLUB: VLSI - transfer to transformation

FEEDBACK ON (Mention the topic): VISI - transistor to transformation DATE: 09/02/2019 Instruction: Please put a tick mark at the appropriate column.

Rating	Clarity	Visuals	Skills	Guidance	Orranall
Excellent	1			Guigance	Overall
Good					
Average				*	
Satisfactory			18		-

Comments/Remarks/Suggestions:

1. It was really good leature on VLSI, and I expect more 2. lectures on these kinds of topics.

3.

Name & USN No.(optional)

Crust lecture

#### NAME OF THE EVENT/CLUB:

FEEDBACK ON (Mention the topic): VLSI\_Transitor toqueting DATE: 9 -02-2019 Instruction: Please put a tick mark at the appropriate column.

Rating	Clarity	Visuals	Skills	Guidance	Overall
Excellent			511110	Guiçance	Overall
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Comments/Remarks/Suggestions:

1,

2.

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Name & USN No.(optional)

NAME OF THE EVENT/CLUB: VLSI - Transiston to transformation

FEEDBACK ON(Mention the topic):

DATE: 11/02/19

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NAME OF THE EVENT/CLUB: VLSI - Transistor to Transformation

FEEDBACK ON(Mention the topic):

DATE: 09-02-2019

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Comments/Remarks/Suggestions:

Very informative, would have been more interactive if it was a maning Version

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Name & USN No.(optional)

VLSI- Transistor to Transformation

Speaker: Mr. Sriram, Intel Corporation

Technology has evolved exponentially over the last century, from the invention of the 1st transistor in 1947 to having several billion transistors on a single chip today, all in accordance to Moore's Law.

Over the years, technology progressed from Small scale integration to medium scale integration to large scale integration and we currently are in the very large scale integration era. This term was coined over 40 years ago though we pushed the size a transistor even further down.

History of Integration

Jack Kilby of Texas Instruments patented the principle of integration, created the first prototype ICs and commercialized them.

Kurt Lehovec of Sprague Electric Company invented a way to electrically isolate components on a semiconductor crystal.

Robert Noyce of Fairchild Semiconductor invented a way to connect the IC components (aluminium metallization) and proposed an improved version of insulation based on the planar technology by Jean Hoerni.

FinFET Technology

Standard 32nm MOSFETs were the predecessors of the FinFETs. The MOSFETs were now large and to keep up with Moore's Law, the FinFETs were developed. The FinFETs that are present in Apple's A12 Bionic chip uses the 7nm technology. The term 7nm used to once describe the width of the channel but in today's context, 7nm indicates the degree of precision achievable or the smallest change that can be made inside the transistor.

The challenge to keep up with Moore's Law is ever growing the technology today is so sophisticated that our transistors are close to the size of a single Si atom i.e., 0.23nm. Intel is currently working with the 7nm technology, along side research to shrink the size of the transistor even further down.

VLSI design flow

Speaking of a billion 7nm transistors on a 3cm x 3cm chip, how is it actually done?

This process can be classified into 2 main blocks, Design and Synthesis.

In Depth, there are 10 steps in fabricating an Integrated Chip

- 1. Design Entry- Designing the model in a HDL design environment using VHDL or Verilog.
- 2. Logic Synthesis- Converting the design to a Gate Level Diagram
- 3. System Partitioning- Dividing the existing blocks of the design into smaller blocks
- 4. Pre-layout Simulation- To simulate the circuit, check the layout and obtain a desired output.
- 5. Floor Planning- assigning different blocks a specific place on the chip

- 6. Placement- Placing these blocks on the chip
- 7. Routing- Connecting these blocks and isolating the metal layers
- 8. Circuit Extraction- Removing additional and other parasitic elements.
- 9. Post Layout simulation- Testing the design
  - 10. Synthesis- Implementing the design on an actual Si Chip

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