NEW HORIZON COLLEGE OF ENGINEERING

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

23/08/2019

GUEST LECTURE

This is to inform to V semester students of ECE that the guest lecture is arranged on 24/08/19 at Chanakya Seminar Hall between 2.00 PM to 4.00 PM.

Topic to be delivered	:	VLSI Design.
Name of the Speaker	:	Tabassum V Mulla.
Designation	:	Senior Member of Technical Staff
Company	:	Invecas, Bangalore.

Respective subject teachers are hereby informed to be present at Chanakya Seminar Hall during the lecture.

All the faculty members are invited to attend the same without affecting the regular classes.

Guest Lecture Coordinator

HOD-ECE

Tabassum V Mulla
Bangalore, India

Phone+918105792479
Email: tabu.mulla@gmail.com

Profile Summary

12+ years of professional IT experience in **VLSI field** and Experience in **Standard Cell Library development.**

Work Experience Summary

- **Invecas**, Bangalore,India
  - Designation : Senior Member of Technical Staff
  - Currently working

- **ARM Embedded Technologies**, Bangalore,India
  - Designation : Senior Layout Designer
  - Worked from : Jan 2014 till March 2016

- **Masamb Electronics**, Bangalore, India
  - Designation :Lead Design Engineer
  - Worked from : Dec 2012 till Dec 2013
  - Worked for designated client like **Texas Instruments.**

- **Karmic**, Bangalore, India
  - Designation : Member of Technical staff
  - Worked from : July 2006 till Dec 2012.
  - Worked for designated clients like **Texas Instruments and Qualcomm.**

Experience Summary

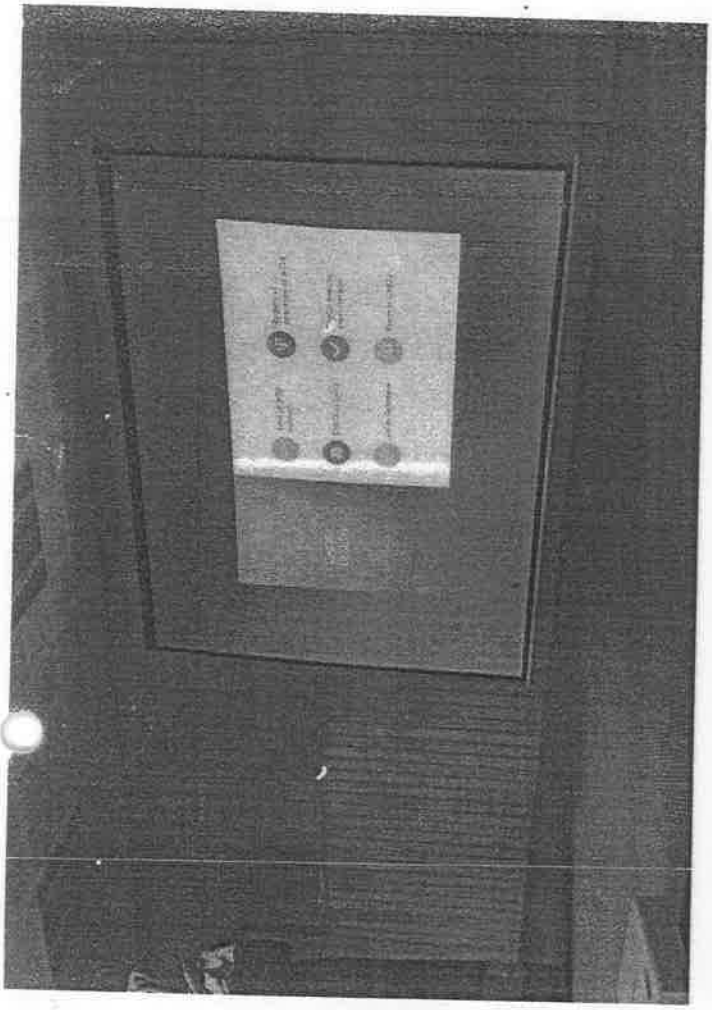
- Expertise in Standard Cell Libraries development (schematic , layout , library integration , complete back end package) at **20nm ,45m, 65nm and 120nm.**
- Expertise in Standard Cell Libraries development in FinFet and FDSOI technologies
- Schematic Design and Simulation for standard cells using hspice,TI-spice.
- Insightful experience in defining cell layout architecture for standard cells.
- Work Experience in cell characterization flow.
- Work experience in building an automated system for library quality using perl and skill scripting .
- Experience in verification of Verilog models .
- Excellent in project implementation, team interaction.
- Strong communication skills with good team spirit.
- Ability to adapt to new environment, highly self motivated and goal oriented.

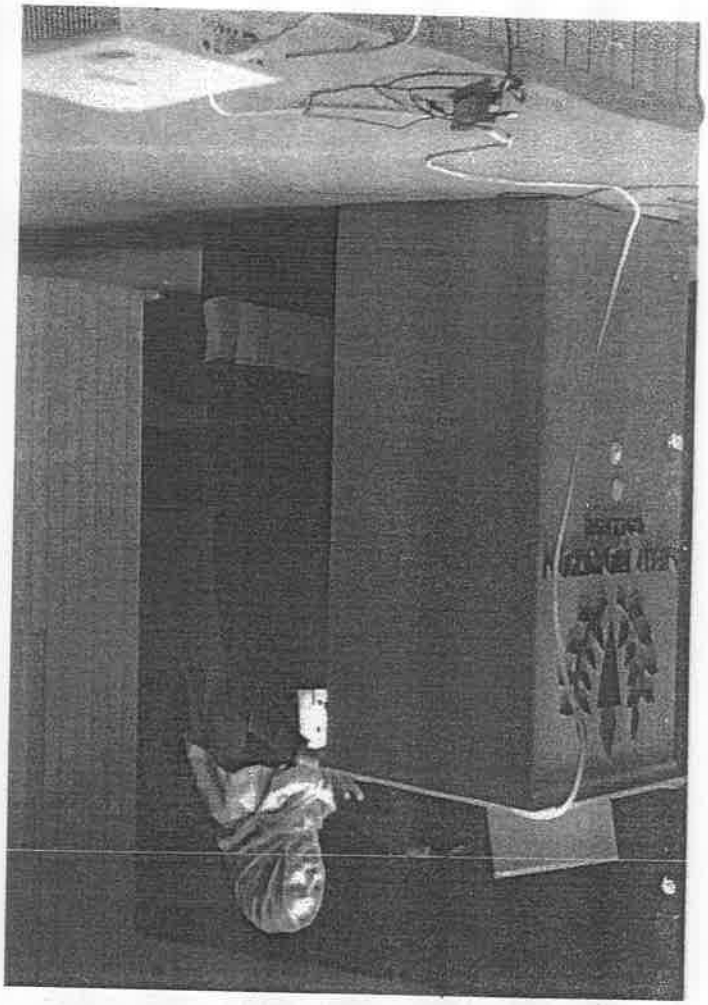
Technical Skills

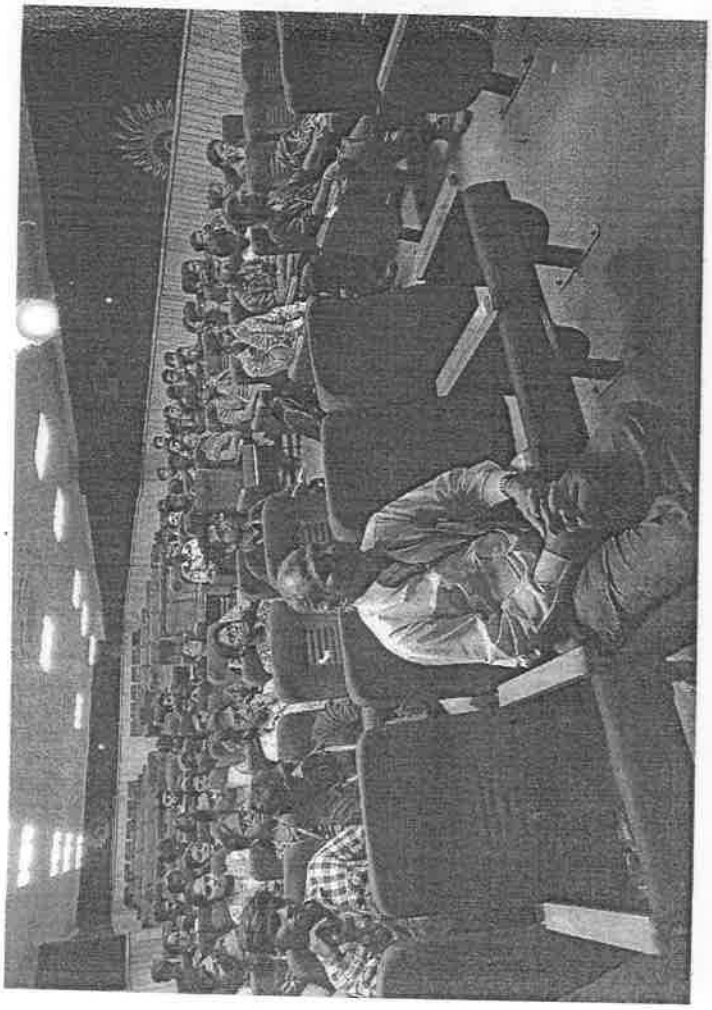
- **Layout tools:** Cadence Virtouso layout Editor.
- **Schematic capture and simulation tools:** Cadence schematic editor.
- **Simulation tools:** Spice3 (TI-spice),Hspice
- **Physical Verification tools:** Plato, K2 Ver,Calibre
- **Operating Systems:** Microsoft Windows, Linux, Design-Sync (Solaris) and Unix.
- **Programming Skills:** Skill, Perl, Shell and know other languages C.
- **Application Software:** MS-office, excel, word, Clearcase, Design-sync.
- **Data formats known:** LEF, GDSII, .lib(CCS and NLM), LAEF, Cad Views
- **HDL:** Basic understanding of Verilog and VHDL.

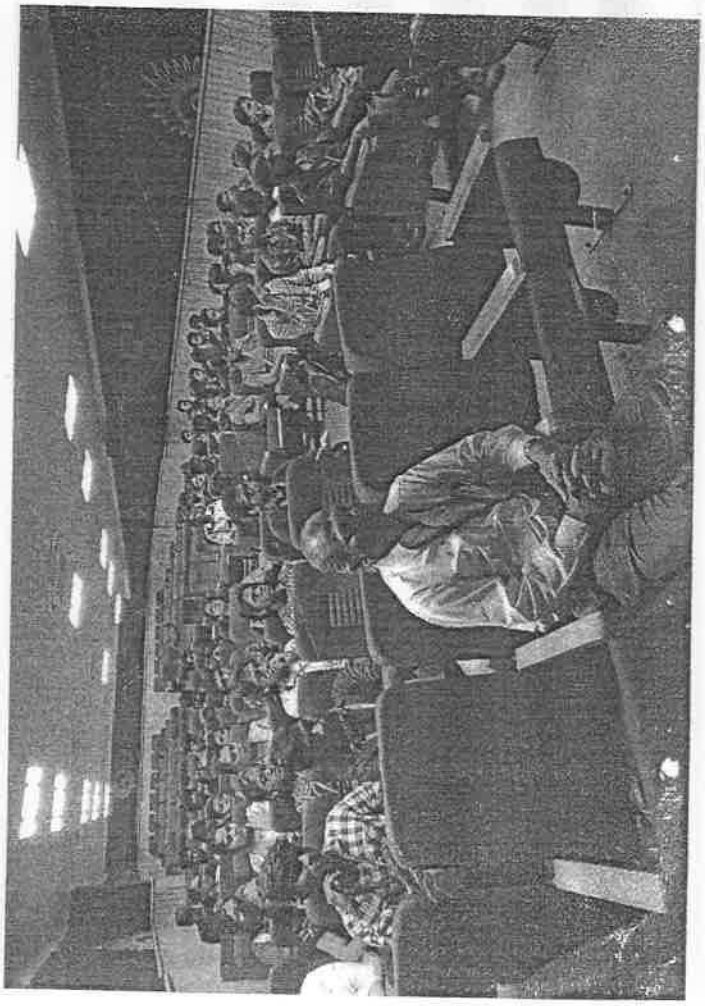
Educational Details:

Degree and Date	Institute	Major and Specialization	Percentage Scored
Bachelor of Engineering, June 2006	B.V.B College of Engineering, & Tech., Hubli.	Electronics and communication	80 % (Aggregate)
PUC II, April 2002	P.C.Jabins Science College, Hubli	PCMB	96.00%(PCM) 86%(Aggregate)
SSLC , March 2000	St.Michaels High School, Hubli		91.00%









NEW HORIZON COLLEGE OF ENGINEERING
DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING
V Sem "A" Sec

SL.No	USN	NAME	Stream	Batch	Dated
1	1NH14EC015	AMUDHA G (Rejoinee)	EXE	A2	
2	1NH16EC013	BOMMI REDDY YUGANDHAR REDDY (Rejoinee)		A3	
3	1NH16EC027	ELDHO JOSE (Rejoinee)		A3	
4	1NH17EC002	ADESH V	PROF	A1	
5	*1NH17EC003*	*ADITYA OMPRAKASH CHOUDHARY*	*EXE*	*A1*	
6	1NH17EC004	AKSHITHA R	EXE	A1	
7	1NH17EC005	ANAND T	EXE	A1	
8	1NH17EC006	ANAND T	PROF	A1	
9	1NH17EC007	ANKIT KUMAR	EXE	A1	
10	1NH17EC008	ARUN Y S	EXE	A1	
11	1NH17EC009	B S ABHISHEK	EXE	A1	
12	*1NH17EC010*	*B YAMINI*	*EXE*	*A1*	
13	1NH17EC011	BHARATH M	PROF	A1	
14	1NH17EC012	BHARATH Y R	EXE	A1	
15	1NH17EC013	BHASKAR K	EXE	A1	
16	***1NH17EC014***	***BOGGARAPU MOURYA YASWANTH***	***EXE***	***A2***	
17	*1NH17EC015*	*BOREDDY NAGA MAHESWAR*	*EXE*	*A2*	
18	1NH17EC016	C O PRUTHVI	EXE	A2	
19	1NH17EC018	CHETHAN B R	PROF-G	A2	
20	***1NH17EC019***	***DEEKSHITH N REDDY***	***PROF-G***	***A2***	
21	1NH17EC021	DEVASHRUTHA S	PROF	A2	
22	*1NH17EC022*	*DHANYASHREE V REDDY*	*EXE*	*A2*	
23	1NH17EC023	DIVYA SAGAR REDDY	EXE	A2	
24	*1NH17EC026*	*G R VARSHA*	*EXE*	*A2*	
25	1NH17EC027	GAGAN B K	EXE	A2	
26	1NH17EC028	GAUTAM SINHA	EXE	A2	
27	1NH17EC030	H K BHASKAR	EXE	A2	
28	1NH17EC031	HARSHITHA G	EXE	A2	
29	1NH17EC032	IVATURI S S HARSHAVARDHAN	EXE	A2	
30	1NH17EC033	J RUTH SHARON	EXE	A2	
31	1NH17EC034	JERIN JOHNSON	EXE	A2	
32	***1NH17EC035***	***JITENDER***	***EXE***	***A2***	
33	1NH17EC036	K S SIRISH	PROF	A2	
34	1NH17EC037	K S SNEHA LATHA	EXE	A2	
35	1NH17EC038	KARAN SRINIVAS	EXE	A3	
36	*1NH17EC039*	*KAVYASHREE S*	*EXE*	*A3*	
37	*1NH17EC040*	*KEVINE PRASANNA KUMAR*	*PROF-G*	*A3*	
38	1NH17EC041	KUSHALA C	EXE	A3	
39	1NH17EC042	M BHARAT	EXE	A2	
40	*1NH17EC043*	*M HEMANTH YADAV*	*EXE*	*A3*	
41	1NH17EC044	MADALA HIMAJA	EXE	A3	
42	1NH17EC045	MADHUMITHA R	EXE	A3	

43	1NH17EC046	MADHUPARNA BANERJEE	PROF	A3	
44	1NH17EC047	MAMATHA B S	EXE	A3	
45	1NH17EC048	MANIKANTA	PROF	A3	
46	1NH17EC049	MANISH B	PROF	A3	
47	**1NH17EC051**	**MILAN SHANKAR RAO M**	**EXE**	**A3**	
48	1NH17EC052	MOHAMMED GHASSAN	PROF	A2	
49	1NH17EC053	MONIKA K REDDY	EXE	A3	
50	1NH17EC054	NANDURI SRILASYA	EXE	A3	
51	**1NH17EC055**	**NAVAJITH R REDDY**	**EXE**	**A3**	
52	1NH17EC056	NAVEEN K M	EXE	A3	
53	1NH17EC057	NETTEM PARNITHA	EXE	A3	
54	1NH17EC058	NIKITH BABU	EXE	A3	
55	**1NH17EC127**	**SUMAN PAL**	**EXE**	**A1**	
56	1NH17EC128	SUHAIL PASHA	EXE	A1	
57	1NH17EC129	BATHULA SRI SAI KRISHNA	EXE	A1	
58	1NH17EC130	ANISHA DEVI	EXE	A1	
59	**1NH17EC131**	**ASHWIN S P**	**EXE**	**A3**	
60	1NH17EC132	MURAKONDA AVINASH	EXE	A1	
61	1NH17EC133	THURPUNATI SURYA PRAKASH	EXE	A1	
62	1NH17EC135	SAI KARTHIK P R	PROF	A1	
63	1NH17EC137	GANGADHARA VARSHITHA	PROF	A1	
64	**1NH18EC405**	**Charan S**	**Prof**	**A3**	
65	1NH18EC407	Nagesh N Reddy	Prof	A1	
66	1NH18EC408	Pragati Shrinivas Naik	Prof	A1	
67	1NH18EC409	Prashant Joshi	Prof	A3	
68	**1NH18EC410**	**Ravi S**	**Prof**	**A3**	
69	**1NH18EC414**	**Santosh B Gonal**	**Prof**	**A2**	
70	**1NH18EC417**	**Spoorthi S T**	**Prof**	**A1**	
71	1NH18EC418	Swaroop M R	Prof	A1	
72	**1NH18EC421**	**Vinod K**	**Prof**	**A1**	
73	1NH18EC422	Yashwanth N K	Prof	A2	
74	1NH18EC424	Naveen N	Prof	A3	
75	1NH18EC425	Nikhil Gopal Krishna Sirsikar	Prof	A3	
76	1NH18EC428	Sandeep Reddy V	Prof	A2	
77	1NH18EC432	Vishal Nayak	Prof	A1	

1NH17EC015 ARUDHAS

HOD - ECE

NEW HORIZON COLLEGE OF ENGINEERING
DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING
V Sem "C" Sec

SL.No	USN	NAME	Stream	Batch	Dated
1	1NH16EC136	ALVIRA SUZANA (REJOINEE)	PROF	C1	
2	1NH16EC701	A NAVYA SHREE	EXE	C3	
3	1NH17EC420	Prathamesh Kadam (Rejoinee)		C3	
4	*1NH17EC700*	*AATHIRA VIJAYAN*	*EXE*	*C1*	
5	1NH17EC701	AJAY S	EXE	C1	
6	1NH17EC702	AKSHAJA SHIMALNA O K	EXE	C1	
7	1NH17EC703	ARAVIND P M	PROF	C1	
8	1NH17EC704	ASHIKA P	EXE	C1	
9	***1NH17EC705***	***BHARGAVI***	***EXE***	***C1***	
10	1NH17EC706	CHANDU V J	PROF-G	C1	
11	1NH17EC707	DHANUSH S	EXE	C1	
12	1NH17EC708	DHINAKARAN S	EXE	C1	
13	1NH17EC709	DISHANTH M P	PROF	C1	
14	1NH17EC710	G DEEPIKA	EXE	C1	
15	*1NH17EC711*	*GAGANASHREE P S*	*EXE*	*C1*	
16	1NH17EC712	GRACE GLADYS A	EXE	C1	
17	1NH17EC713	HARSHITH NAIDU J	EXE	C1	
18	1NH17EC714	J BHAVANA	EXE	C1	
19	*1NH17EC715*	*JAYADEEP G P*	*EXE*	*C1*	
20	***1NH17EC716***	***JILLELLA RUPASAGAR REDDY***	***EXE***	***C1***	
21	*1NH17EC717*	*K AISWARYA*	*EXE*	*C1*	
22	1NH17EC718	KONDURU SIVARAMA RAJU	EXE	C1	
23	*1NH17EC720*	*LAVANYA S N*	*EXE*	*C2*	
24	*1NH17EC721*	*MANISHA M N*	*EXE*	*C2*	
25	1NH17EC722	MANOHAR G	EXE	C2	
26	***1NH17EC723***	***MANOJ M R***	***PROF***	***C2***	
27	*1NH17EC724*	*MUNAGALA BHARATH KUMAR REDDY*	*EXE*	*C2*	
28	1NH17EC725	NAINI NARAMA	EXE	C2	
29	1NH17EC726	NAVEEN KUMAR M S	EXE	C2	
30	*1NH17EC727*	*NEHA KRISHNA*	*EXE*	*C2*	
31	*1NH17EC728*	*NIDUJUVVI CHAKRADHAR*	*EXE*	*C2*	
32	*1NH17EC729*	*NIKHIL DWIVEDI*	*EXE*	*C2*	
33	1NH17EC730	P K KANAKA SHARANYA	EXE	C2	
34	1NH17EC731	PALVADHI VENKATA SAI PAVAN KALYAN	PROF-G	C2	
35	***1NH17EC732***	***PAVAN U***	***EXE***	***C2***	
36	1NH17EC733	PRACHI VERMA	PROF	C2	
37	1NH17EC734	PRAJWAL P	EXE	C2	
38	1NH17EC736	RAHUL BALAJI P S	EXE	C2	

39	1NH17EC737	RISHIKA POTEPALLI	EXE	C2	
40	1NH17EC738	RITWIK SHOME	PROF	C2	
41	1NH17EC739	S DENILA GRACELIN	EXE	C2	
42	1NH17EC740	S RAHUL YADAV	EXE	C2	
43	1NH17EC742	SAHIB ARORA	EXE	C3	
44	1NH17EC743	SANDHYA K	EXE	C3	
45	1NH17EC744	SHARATH T P	PROF	C3	
46	1NH17EC745	SHARON MOSES	PROF-G	C3	
47	1NH17EC746	SHASHANK REDDY J	EXE	C3	
48	1NH17EC747	SHASHANK S SALOTAGI	PROF	C3	
49	1NH17EC748	SHIVANG DUBEY	EXE	C3	
50	1NH17EC749	SIRISHA B S	EXE	C3	
51	*1NH17EC750*	*SOMA YASWANTH REDDY*	*EXE*	*C3*	
52	***1NH17EC751***	***SREEKAR REDDY KALLAM***	***EXE***	***C3***	
53	1NH17EC752	SUHAS S	EXE	C3	
54	*1NH17EC754*	*THUMMALA SURYA DEVI VARAPRASAD*	*EXE*	*C3*	
55	1NH17EC755	USTHEPALLI ABHIRAM	EXE	C3	
56	1NH17EC756	VARUN P	PROF	C3	
57	1NH17EC758	Y SUCHARITHA	EXE	C3	
58	***1NH17EC759***	***YERRABALLI GURU SAI KUMAR***	***EXE***	***C3***	
59	1NH18EC402	Aiyappa K K	Prof	C3	
60	*1NH18EC406*	*Harshitha M*	*Prof*	*C3*	
61	*1NH18EC411*	*Roja Parameshwar Ullikashi*	*Prof*	*C3*	
62	*1NH18EC419*	*Tejaswini T R*	*Prof*	*C3*	

HOD - ECE

NEW HORIZON COLLEGE OF ENGINEERING
DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING
V Sem "B" Sec

SL.No	USN	NAME	Stream	Batch	Dated
1	1NH16EC074	PAVAN KUMAR S (Rejoinee)		B1	
2	1NH16EC111	VEDA MILIND (Rejoinee)	EXE	B3	
3	1NH17EC060	NISHMITHA C SHETTY	EXE	B1	
4	1NH17EC062	NITHIN R KALLIGUDI	EXE	B1	
5	1NH17EC063	PALAGIRI JYOTHI KRISHNA	EXE	B1	
6	1NH17EC064	PANUGANTI VIKAS	EXE	B1	
7	*1NH17EC065*	*PARTHASARATHI N*	*EXE*	*B1*	
8	1NH17EC066	PASSAVULA PHANINDRA	EXE	B1	
9	1NH17EC068	PRANAY CHATURVEDY	EXE	B1	
10	1NH17EC069	PRAVEEN KUMAR S	EXE	B1	
11	1NH17EC070	PREETHU C	EXE	B1	
12	1NH17EC071	PRINCE CHAURASIYA	PROF	B1	
13	*1NH17EC072*	*PUNEETH REDDY V*	*EXE*	*B1*	
14	1NH17EC073	R BARATH	EXE	B1	
15	1NH17EC074	R KISHAN KUMAR SAI	EXE	B1	
16	1NH17EC075	R RAGHAVA	PROF-G	B1	
17	*1NH17EC077*	*RAHUL V*	*EXE*	*B1*	
18	*1NH17EC079*	*RENUKA D N*	*EXE*	*B1*	
19	1NH17EC080	RIYA RAKESH	EXE	B1	
20	*1NH17EC081*	*ROHITH P GOWDA*	*EXE*	*B1*	
21	1NH17EC082	RUPSA DATTA	EXE	B1	
22	*1NH17EC083*	*S RISHITA*	*EXE*	*B1*	
23	1NH17EC084	SAIKAT SAMANTA	EXE	B2	
24	1NH17EC085	SAIMANTI SAHA	EXE	B2	
25	1NH17EC086	SAMYUKTHA V	EXE	B2	
26	1NH17EC087	SATEESH R HEGDE	EXE	B2	
27	*1NH17EC088*	*SHAKTHI A*	*EXE*	*B2*	
28	1NH17EC089	SHALINI P N	EXE	B2	
29	1NH17EC090	SHARAN KUMAR K S	EXE	B2	
30	1NH17EC091	SHIVA S	PROF	B2	
31	1NH17EC092	SHOAIB AHMED	EXE	B2	
32	1NH17EC093	SHRESTHA PATNAIK	EXE	B2	
33	1NH17EC094	SHREYANKA S	EXE	B2	
34	*1NH17EC095*	*SHWETA S*	*EXE*	*B2*	
35	*1NH17EC096*	*SOUVIK DAS*	*EXE*	*B2*	
36	1NH17EC097	SOWMIYA A	EXE	B2	
37	*1NH17EC099*	*STANISLAUS LASRADO*	*PROF*	*B2*	
38	*1NH17EC100*	*SUHAIB AFNAN*	*PROF*	*B2*	
39	1NH17EC101	SUHAS H G	EXE	B2	
40	1NH17EC102	SUHAS S P	EXE	B2	
41	1NH17EC103	SUMITHRA V ARADHYA	EXE	B2	
42	1NH17EC104	SUNIL PATIL	PROF	B2	

Name	USN
1. R. Kishan Kumar Sai	1NH17EC074
2. YASEER FAIZ AHMED	1NH17EC125
3. PAVAN.Y.	1NH18EC427
4. Vignesh.R	1NH18EC420
5. Suhas S.P	1NH17EC102
6. Sanjay	1NH18EC413
7. Shoaib Ahmed	1NH17EC092
8. SHIVA S	1NH17EC091
9. Shreekanta	1NH18ECH16
10. Syale Rajkumar	1NH17EC106
11. Partha Sarathi. N	1NH17EC065
12. RAHUL.V	1NH17EC077
13. R. Raghava	1NH17EC075
14. Praveen Kumar.S	1NH17EC069
15. P.Phanindra	1NH17EC066
16. N.Lokesh	1NH17EC139
17. V.Dharanidhar Reddy	1NH17EC113
18. Palagiri Jyothi Krishna	1NH17EC063
19. Thejas.U	1NH17EC109
20. Barath.R	1NH17EC073
21. Shakthi.A	1NH17EC088
22. T.V. Vasan Sai	1NH17EC107
23. Shagan Kumar K.S	1NH17EC090
24. S.Karthik Reddy	1NH17EC138

NEW HORIZON COLLEGE OF ENGINEERING
DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
FEEDBACK FORM

NAME OF THE EVENT/CLUB: CMOS Layout & Design Seminar

FEEDBACK ON(Mention the topic): **DATE:** 24/08/19
Instruction: Please put a tick mark at the appropriate column.

Rating	Clarity	Visuals	Skills	Guidance	Overall
Excellent	✓		✓		
Good		✓		✓	✓
Average					
Satisfactory					

Comments/Remarks/Suggestions:

1. It was a good exposure to the current technology used in the industry but few concepts of MOS have not yet been taught yet for us to understand like the factors affecting delay and noise margin. It would be good if we start with the basics first before getting into the topic.
2.
3.

Name & USN No.(optional)
DEVASHRUTHA.S
1NH17EC021

Signature (optional)
S. Devashrutha

NEW HORIZON COLLEGE OF ENGINEERING
DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
FEEDBACK FORM

NAME OF THE EVENT/CLUB: CMOS Layout design seminars.

FEEDBACK ON(Mention the topic):

DATE: 24-01-19

Instruction: Please put a tick mark at the appropriate column.

Rating	Clarity	Visuals	Skills	Guidance	Overall
Excellent	✓				
Good		✓	✓	✓	✓
Average					
Satisfactory					

Comments/Remarks/Suggestions:

1. It was a good exposure to the technology used
2. in the industry and about FDSOI and FINFETs.
3. It was informative and learn more about it.

Name & USN No.(optional) SHIVA S.

Signature (optional)

NEW HORIZON COLLEGE OF ENGINEERING
DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
FEEDBACK FORM

NAME OF THE EVENT/CLUB: Seminar on CMOS VLSI design layout

FEEDBACK ON(Mention the topic): **DATE:** 24/08/19

Instruction: Please put a tick mark at the appropriate column.

Rating	Clarity	Visuals	Skills	Guidance	Overall
Excellent					
Good	✓		✓		
Average		✓		✓	✓
Satisfactory					

Comments/Remarks/Suggestions:

1. Give more clarity about Industrial side manufacture.
2.
3.

Name & USN No.(optional)

Signature (optional) Lokanya. S. N

NEW HORIZON COLLEGE OF ENGINEERING
DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
FEEDBACK FORM

NAME OF THE EVENT/CLUB: Seminar on CMOS VLSI layout design

FEEDBACK ON(Mention the topic):

DATE: 24/08/19

Instruction: Please put a tick mark at the appropriate column.

Rating	Clarity	Visuals	Skills	Guidance	Overall
Excellent					
Good	✓		✓		✓
Average		✓		✓	
Satisfactory					

Comments/Remarks/Suggestions:

1. Give more information about Industrial side manufacture of CMOS.
2. PPt's are should be ~~leave~~ include with Industry
3. side Visuals like Manufacture of CMOS Picture

Name & USN No.(optional)

Signature (optional) Jayadeep. G.P.

NEW HORIZON COLLEGE OF ENGINEERING
DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
FEEDBACK FORM

NAME OF THE EVENT/CLUB: SEMINAR ON CMOS Layout design

FEEDBACK ON(Mention the topic): **DATE:** 24/8/19

Instruction: Please put a tick mark at the appropriate column.

Rating	Clarity	Visuals	Skills	Guidance	Overall
Excellent					
Good	✓			✓	✓
Average		✓	✓		
Satisfactory					

Comments/Remarks/Suggestions:

1. It was a good exposure, but to most of what we heard today was already known to us, so I ~~think~~ suggest a session begin after understanding what we already know
2. & the seminar must be focused to give us an extra edge over mainstream classroom & learning

Name & USN No.(optional) STANISLAUS LASRADO.

Signature (optional) Stanislaus

NEW HORIZON COLLEGE OF ENGINEERING
DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
FEEDBACK FORM

NAME OF THE EVENT/CLUB: Seminar CMOS VLSI Layout

FEEDBACK ON(Mention the topic): **DATE:** 24-Aug-18

Instruction: Please put a tick mark at the appropriate column.

Rating	Clarity	Visuals	Skills	Guidance	Overall
Excellent	✓		✓	✓	✓
Good	✓	✓			
Average					
Satisfactory					

Comments/Remarks/Suggestions:

1. A good connect between the industry and academia
2. Please don't be discouraged so easily
3.

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Name & USN No.(optional) RIYA RAKESH

Signature (optional) Riya

NEW HORIZON COLLEGE OF ENGINEERING, BANGALORE

(Autonomous College affiliated to VTU, Accredited by NAAC with Grade 'A' & NBA)

Department of Electronics and Communication Engineering

REPORT ON GUEST LECTURE

Topic: BASICS OF VLSI LAYOUT DESIGN

A seminar on CMOS VLSI was conducted on the **24th of August 2019** by Ms Tabassum V Mulla, Senior Member of Technical Staff at Invecas Technologies, Bangalore with over 12 years of experience in the field of VLSI and Standard cell library development with expertise in standard cell library development in FinFETs. Ma'am is supervising the backend package of standard cell projects at Invecas Technologies. Ms Tabassum has also worked for other tech giants like ARM Embedded Technologies, Masamb Electronics and karmic, working for designated clients like Texas Instruments and Qualcomm. Over 50 students from the 5th semester attended this session.

The session was an interconnect between the industry and Academia. Ms Tabassum explained the difficulties that the present industry facing in **leakage currents and slews** in MOSFETS. Along with MOSFET a brief introduction to FinFETs was also given to us. To keep up with Moore's law, the size of the transistor had to be reduced. But at 28 nm, mainstream MOSFETs couldn't be used. So, FinFETs came into existence. FinFETs are 3 dimensional MOSFETs which the gate on 3 sides. This helped reduced the size even further down to the current 11 nm technology. Though the industry has kept us with Moore's Law, there are still problems associated with it like leakage current and static power loss.

Ms Tabassum explained to us why there is a bulk terminal on the MOSs. This is to control the channel along with the gate and to prevent latch-up which is an internal short-circuiting. Ms Tabassum also explained to us why today the layout designers play a key role in the success of a product in the market unlike how it was otherwise a few years ago. This is because a good layout would mean a lower delay compared to poorer layout design. This delay could be a few Pico seconds but, in the market, it makes a huge difference.

Overall, the session was interactive with activities like drawing outputs and estimating values of various parameters. Also, students were given some homework to research further on topics like FDSOI, Latch-up and technology which battery technologies use. Apart from the technicality, the students received tips on how to get into a core company and how to take advance their current knowledge on the subject. This session was organized by Dr Sanjeev Sharma, HoD, Department of Electronics and Communication and Ms. Dharmambal and Ms. Divya Sharma, Department of Electronics and Communication along with the support of Mr.G. Rajesh sir. A hearty thanks to them on behalf of all the students.

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